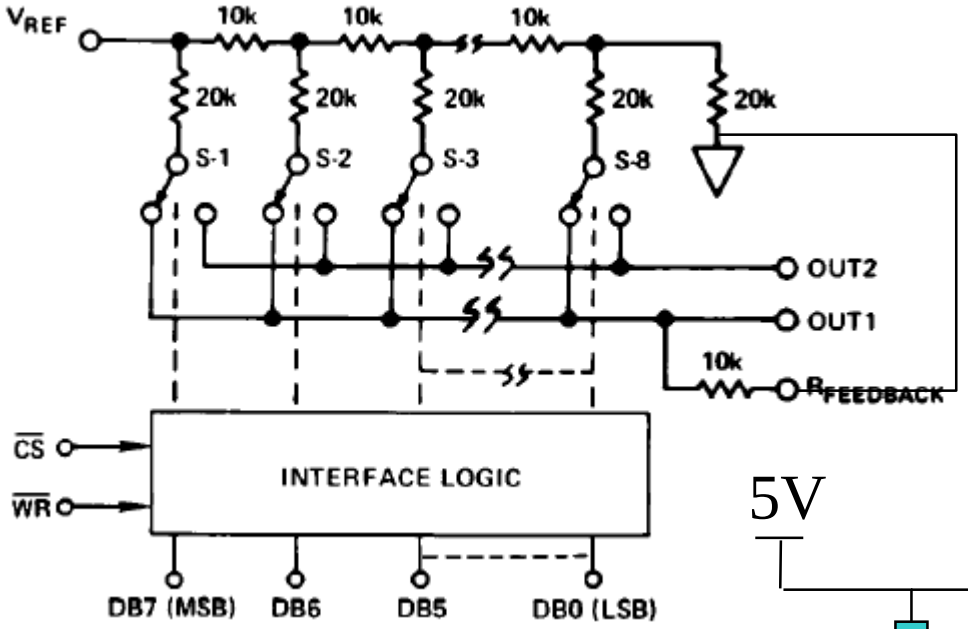
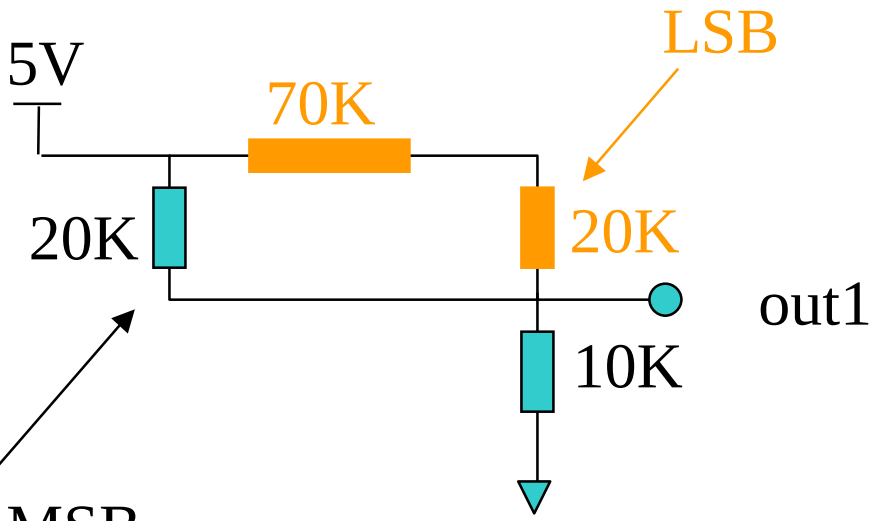
Lab Issues and Questions?

- Daily quiz: How is an interrupt different than a subroutine call?
- Limitations of the assembler
  - Seems to have trouble with SFR access. Stick with Timer 0 for this lab, as suggested by Douglas
  - I know that the simulator does not support Timer 2.
  - Pullup on port – 0

Digital to Analog Converter



each bit pumps more current into Rfb in different amounts depending on position



Effective network is

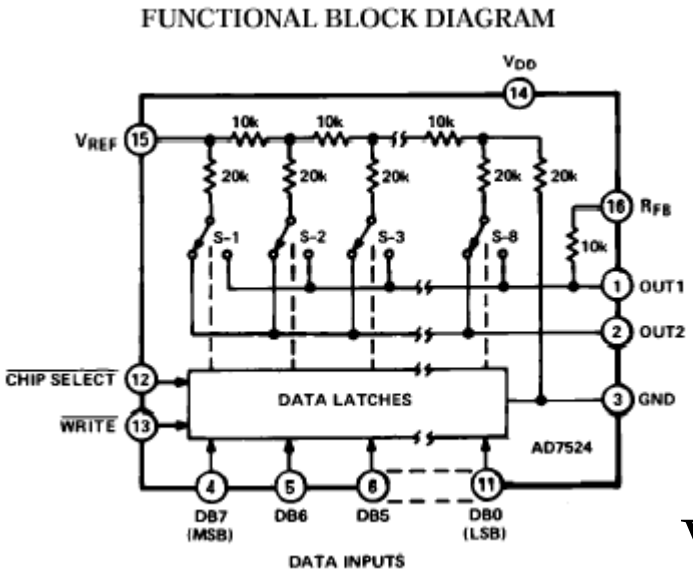
DB[7:0] = 10000000

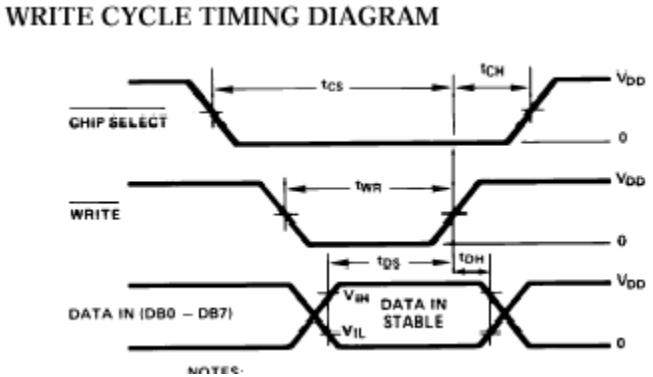
out1 = 10/30 = 0.33Vref

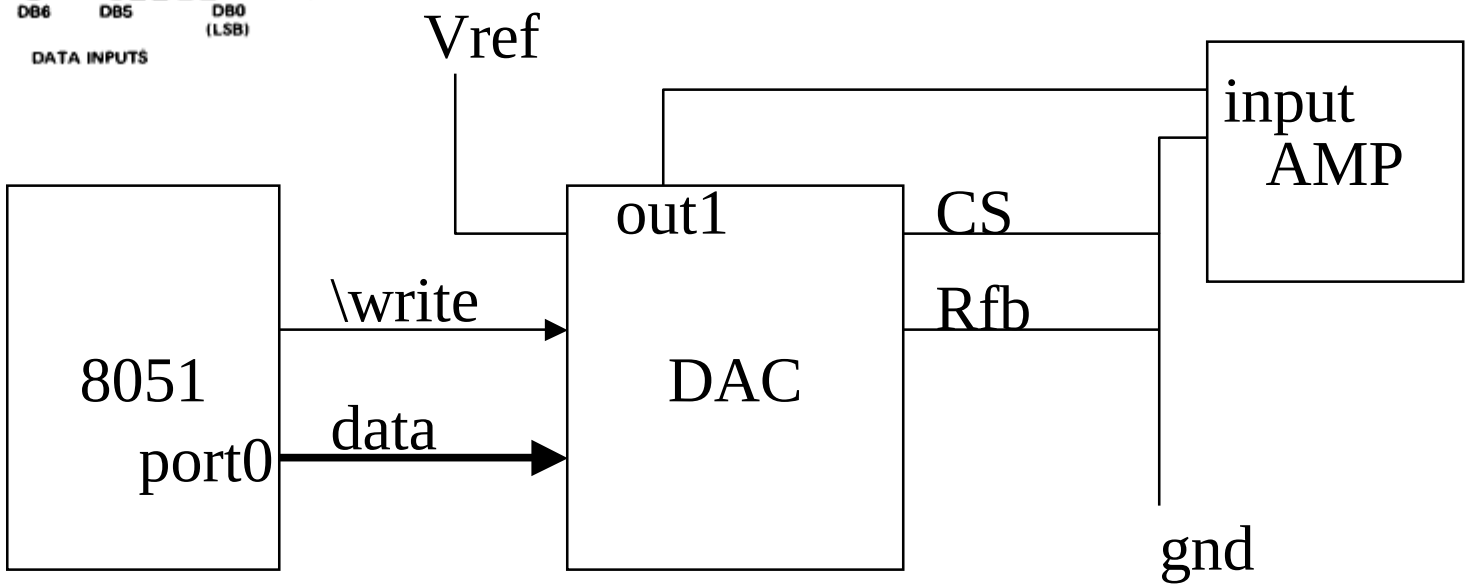
DB[7:0] = 10000001

out1 = 10/(20||90) = 0.38Vref

Digital-to-Analog Converter

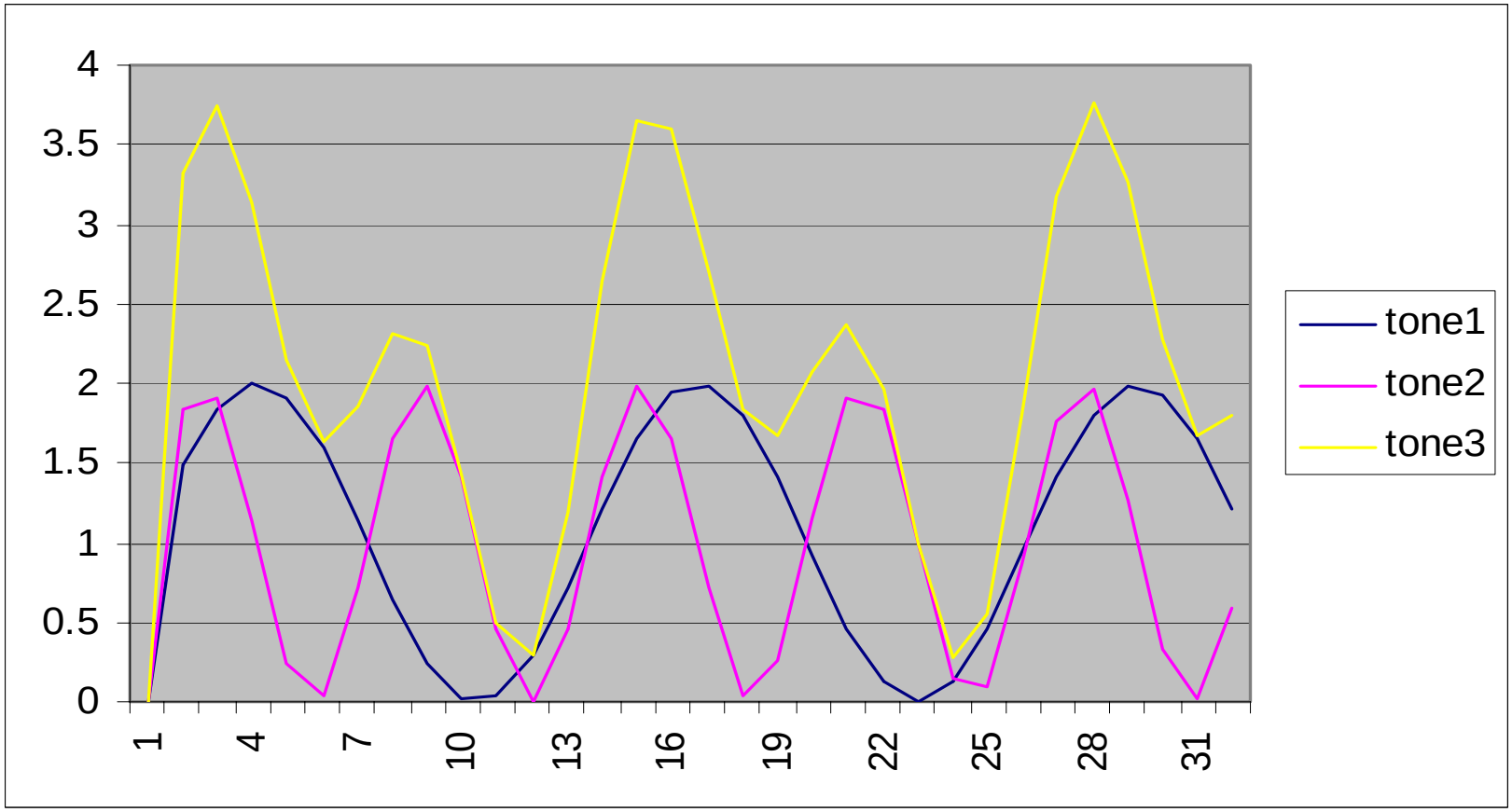






Is Constant Rate Sampling Okay?

- Just like CD player: runs a 44KHz…max frequency it can create is 22KHz,
- A CD recording of a pure 22HKz tone would look like a square/triangle wave on the output of the DAC.



two frequencies with same rate. How fast can you go?

Frequency range w/ fixed sample rate

To get a psuedo-sine wave, what is the max Stride for our lookup table?

- 64: 64/156 (5K) = 1.125KHz

Let Stride = 1 and Sample Rate = 5KHz

- output frequency = 5KHz/256 = 19.531Hz
- low frequencies generate a smoother waveform

Let Stride = n

- output frequency = 5KHz/(256/n) = n*(5KHz/256)

Solve for output frequency

- Stride = (freq*256)/5KHz
- Middle C = 262Hz, so stride = 13.41 can we just round this off? Yes for this week's lab.
- D = 294, so stride = 15.05

What happens for low frequencies

- Low F: 87.31Hz stride = 4.74
- Low E: 82.42Hz stride = 4.47
- what do we do with non-integral strides?

Software Perspective

In software (always through indirect addressing)

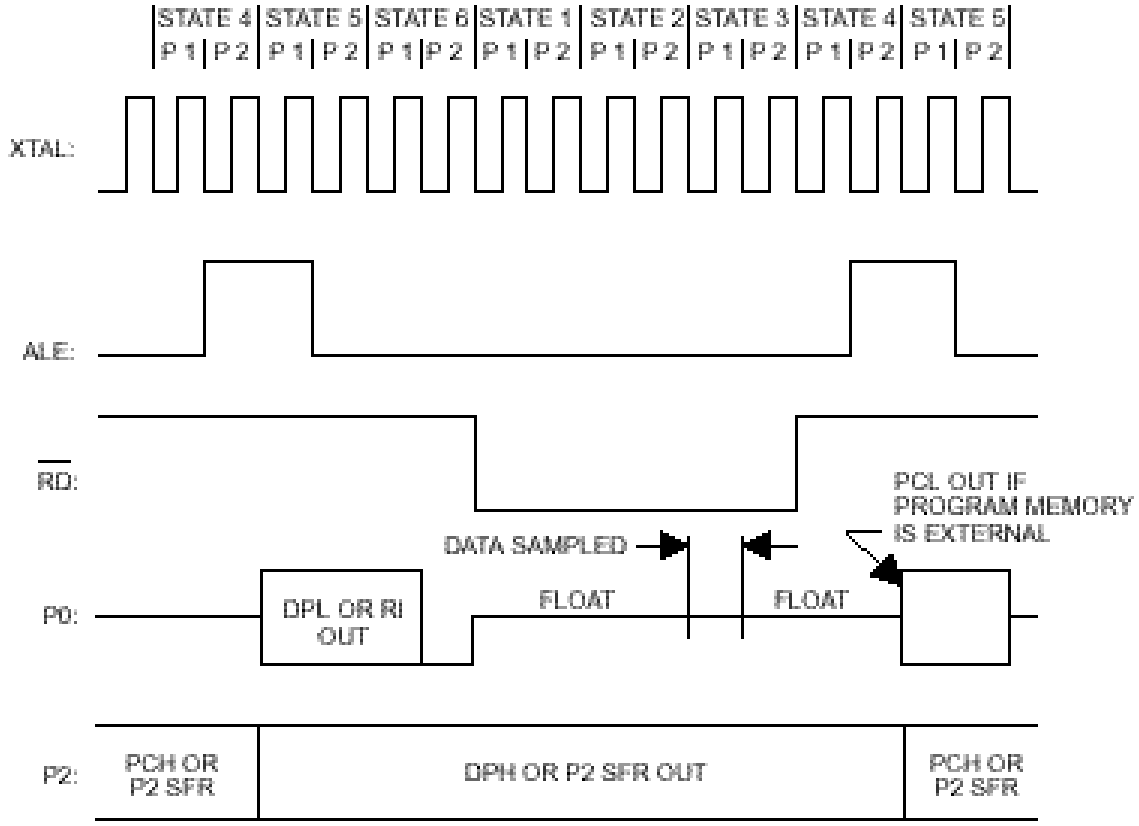
MOV R0, #external_address
MOVX A,@Rx # uses only 8-bit address for external RAM

Or
MOV DPL, #external_address_high
MOV DPH, #external_address_low
MOVX A, @DPTR;
Note that MOVC A, @DPTR references code space

Yet another address space (declare as xdata or pdata)

External Read Cycle

Figure 35. External Data Memory Read Cycle



How fast does
The RAM have to
Be?
7 osc. Cycles
Recall design
Of P0: active pullup
And pulldown so
Data bus can “float”

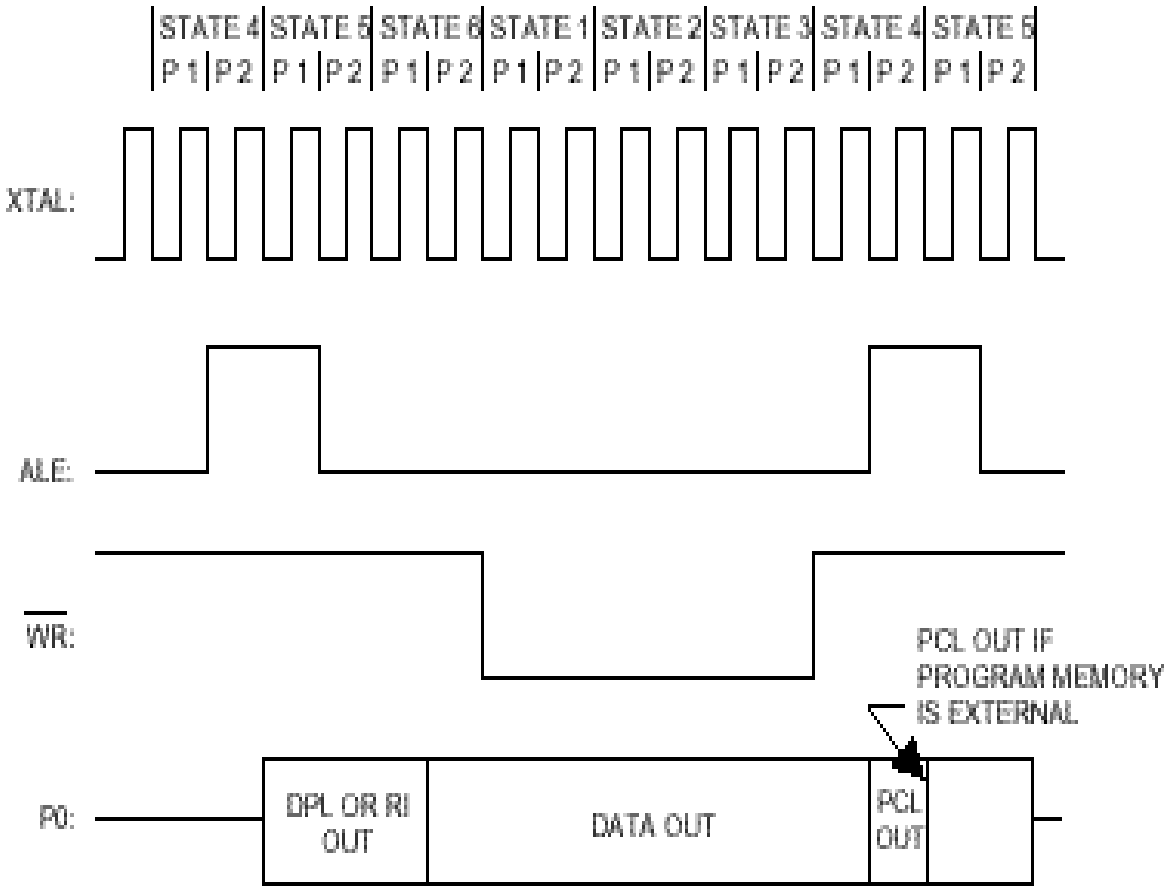
Don’t need pullups
when using P0 as external data bus instead of as regular port

External Memory – Write Cycle

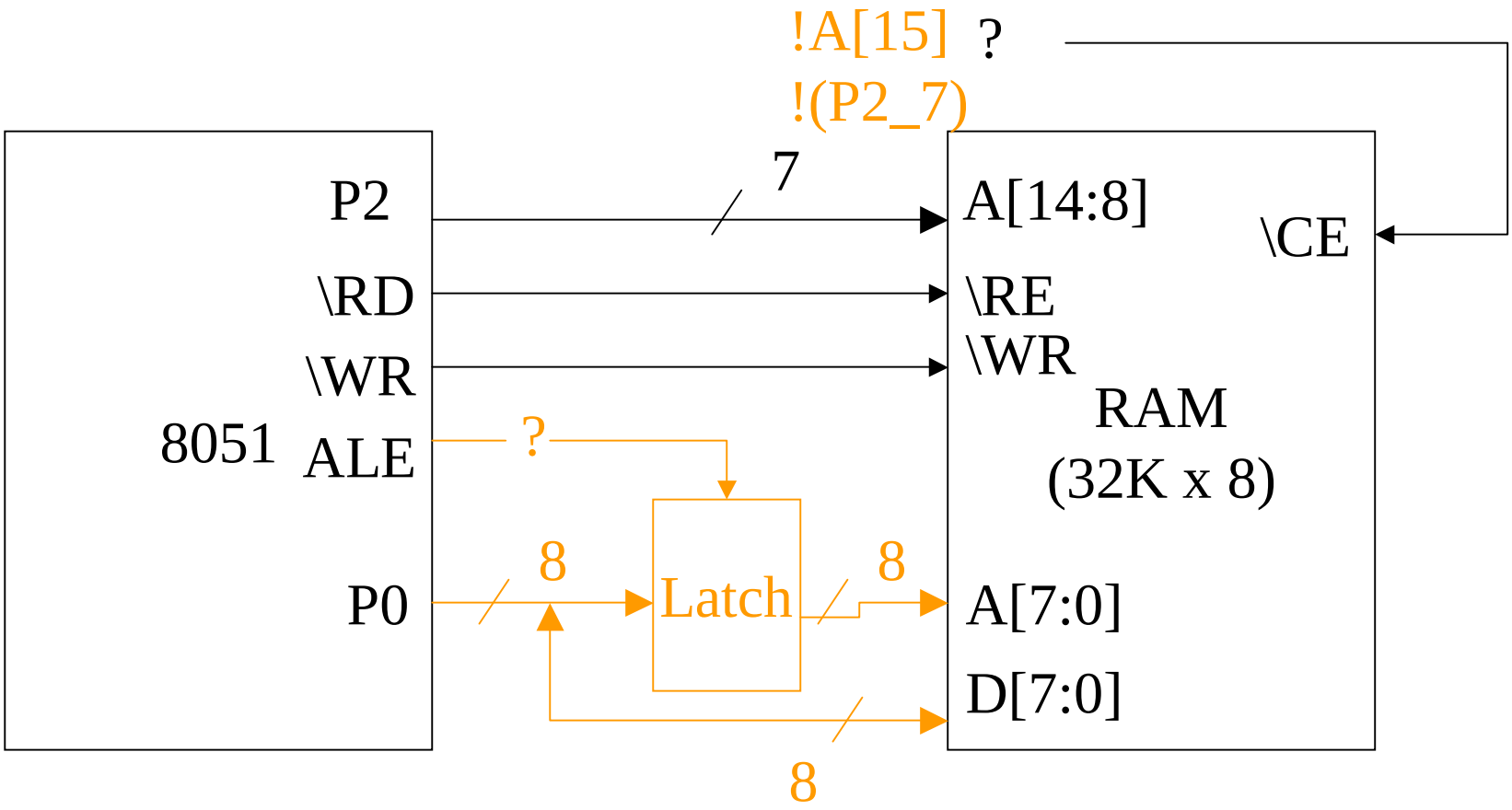
Figure 36. External Data Memory Write Cycle

Multiplex data and Low address on P0 (destroys value on P0)

P2 used for high byte, returns To port value after use.



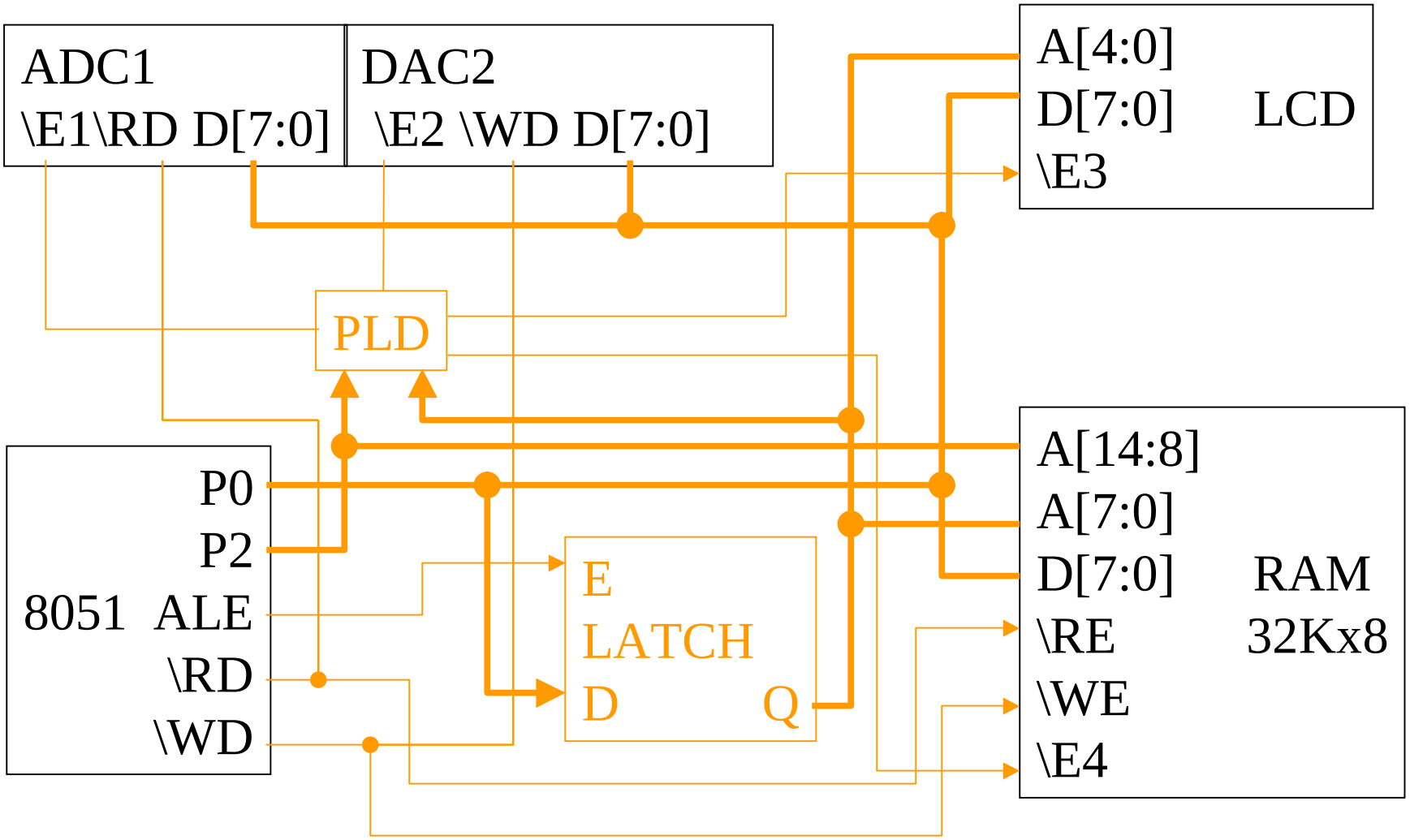
Circuit for external Data Mem.?



Homework:

Draw this schematic and write equations for the logic in the PLD

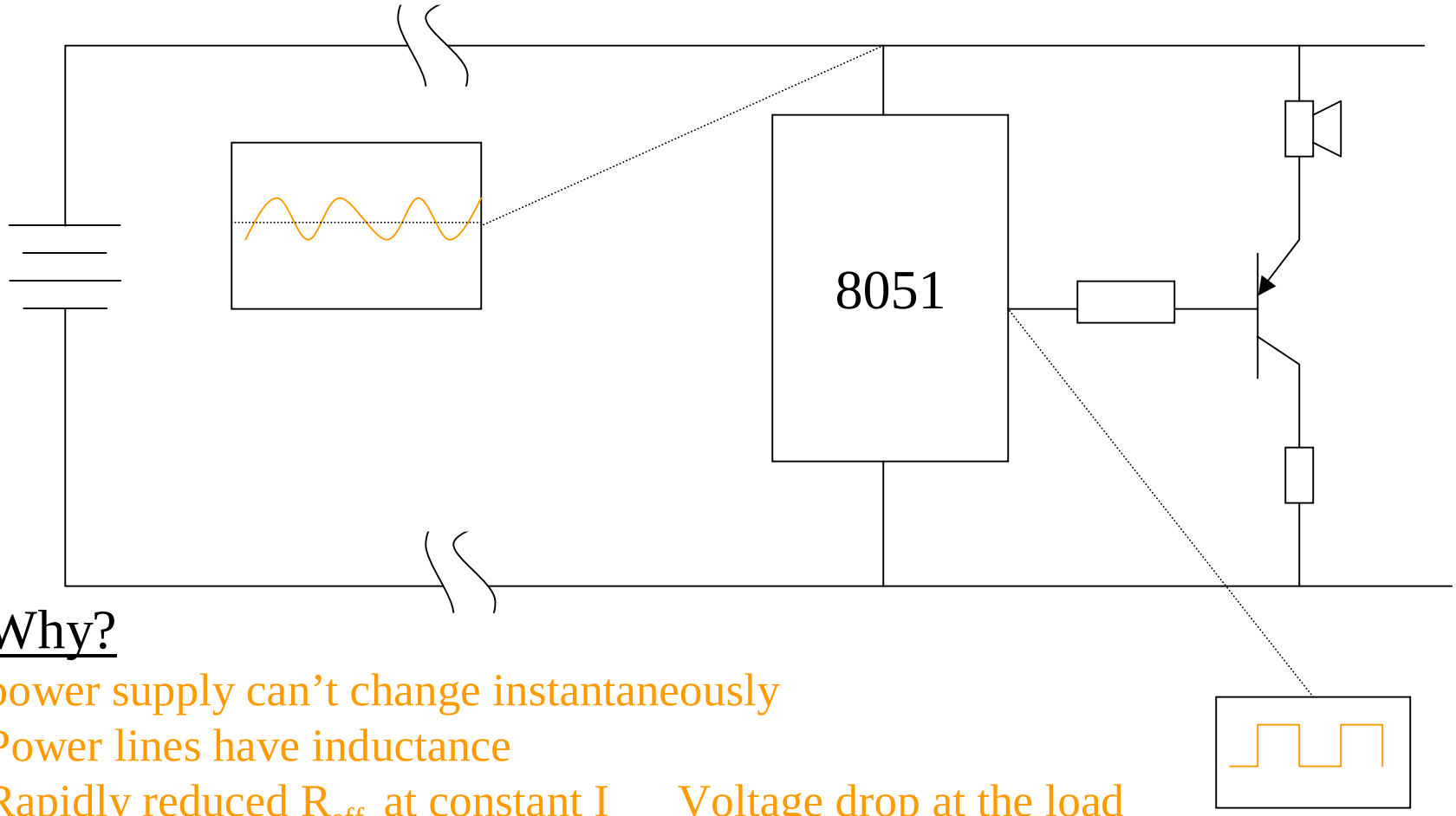
And you thought 370 didn't matter!



Glue Logic Design

1. Define External Memory Map (64K): addr[14:0]
   Ram: Upper 32K enable if address = 1xxxxxxxxxxxxxx
   LCD: 0-31 enable if address = 0xxxxxxx00xxxxx
   DAC2: 32 enable if address = 0xxxxxxx01xxxxx
   ADC1: 64 enable if address = 0xxxxxxx10xxxxx
2. Come up w/ address decoder logic for each case (many to 1 ok, 1 to many not okay!)
   \E4 = (A14)' covers all upper 32K addresses
   \E3 = (A14'A6'A5')' covers 2^12 addresses including 0-31 but excluding upper 32K, 64, 32
   \E2 = (A14'A6'A5)' covers 2^13 addresses but excludes upper 32K, 64, 0-31
   \E1 = (A14'A6A5')' covers 2^13 addresses but excludes upper 32K, 32, 0-31

Power Supply Noise



Why?

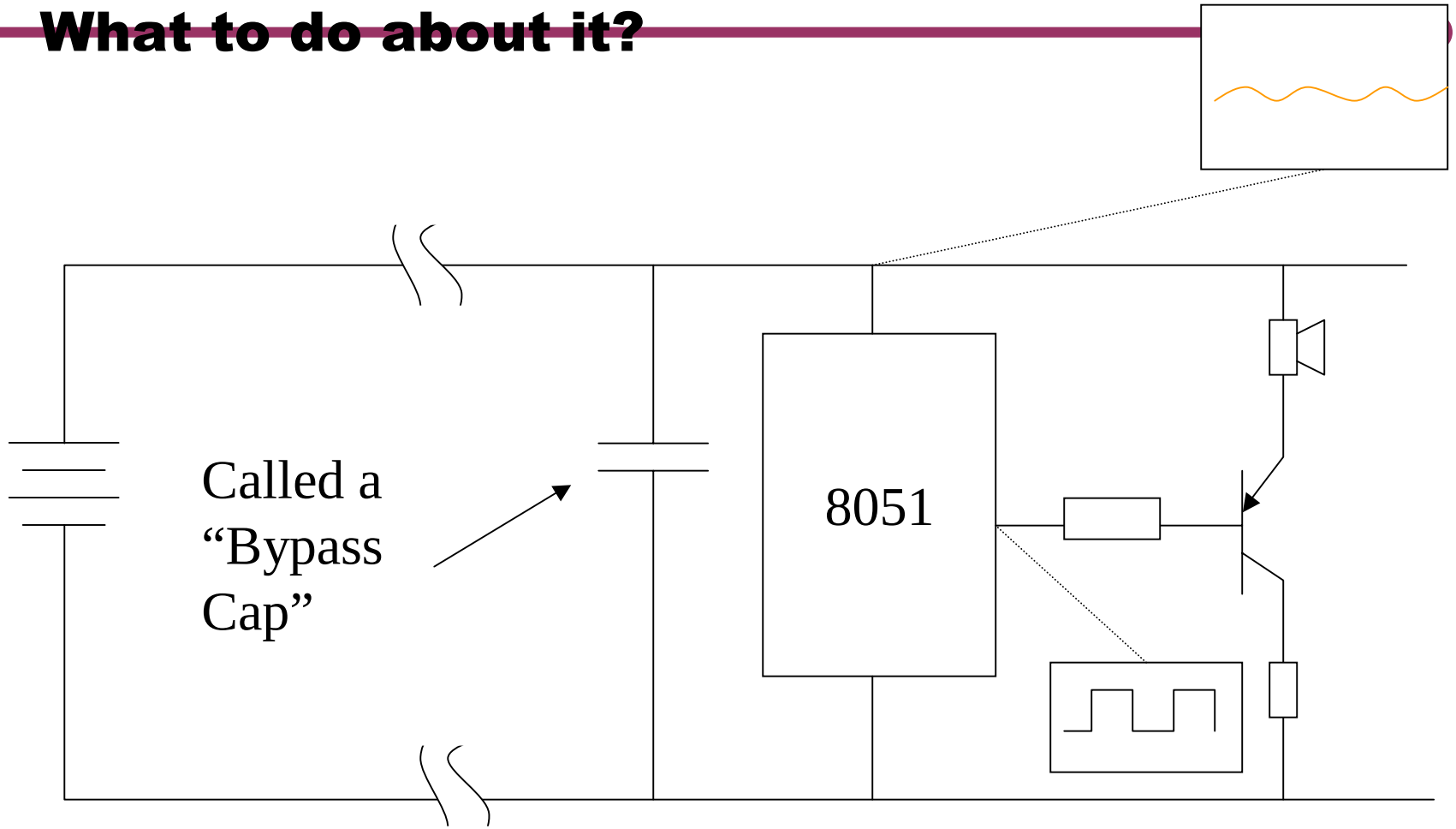
power supply can't change instantaneously

Power lines have inductance

Rapidly reduced R_{eff} at constant I Voltage drop at the load

So what? Could cause processor to reset/go to unknown state, mess up analog voltage readings, cause electromagnetic interference

What to do about it?



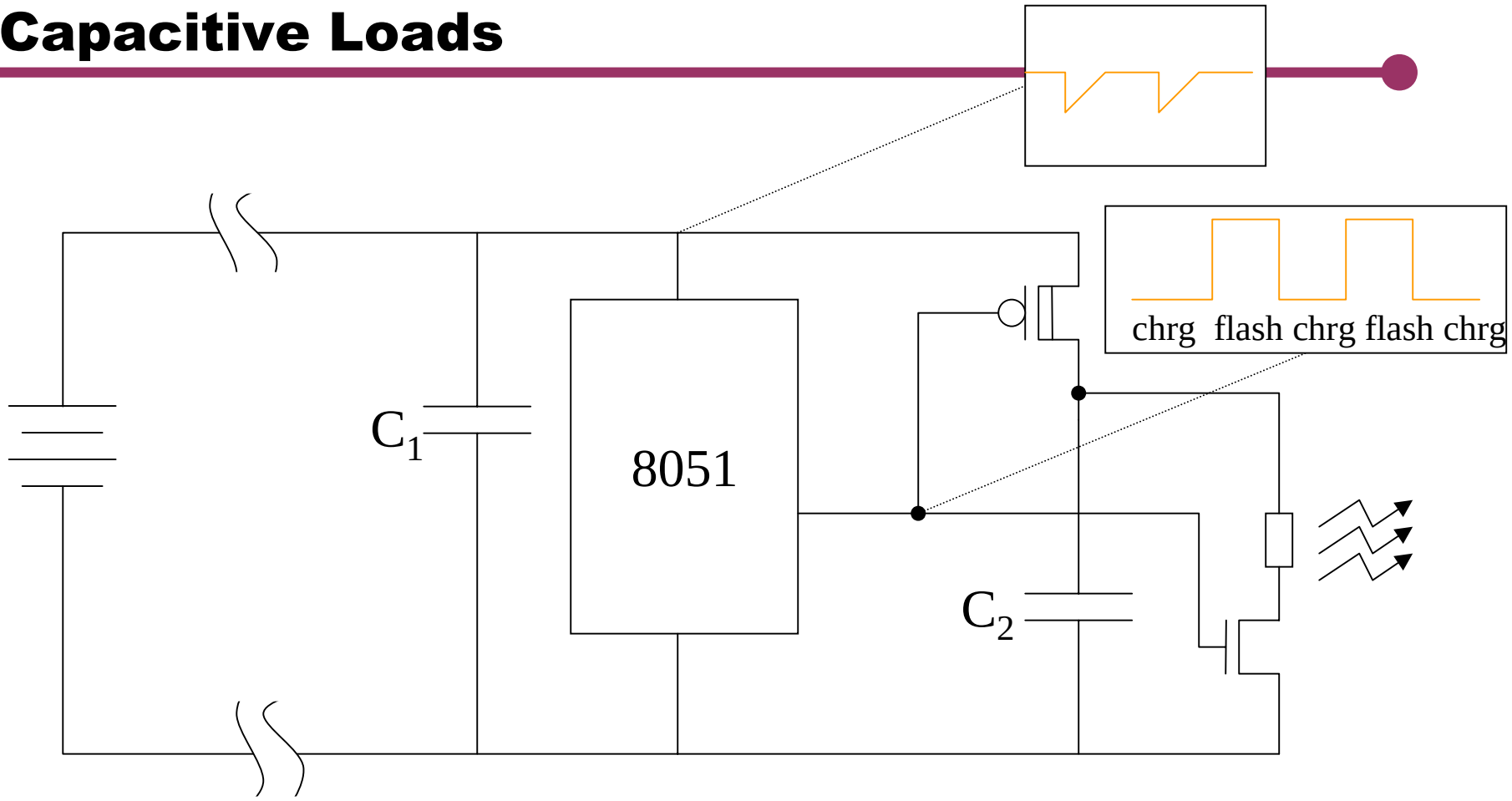
How big should cap be?

Depends on speed and inductance of the supply, and ΔI when switched

Typical values for digital boards are .1uF/IC placed very close to IC

….then there’s capacitive loads….

Capacitive Loads



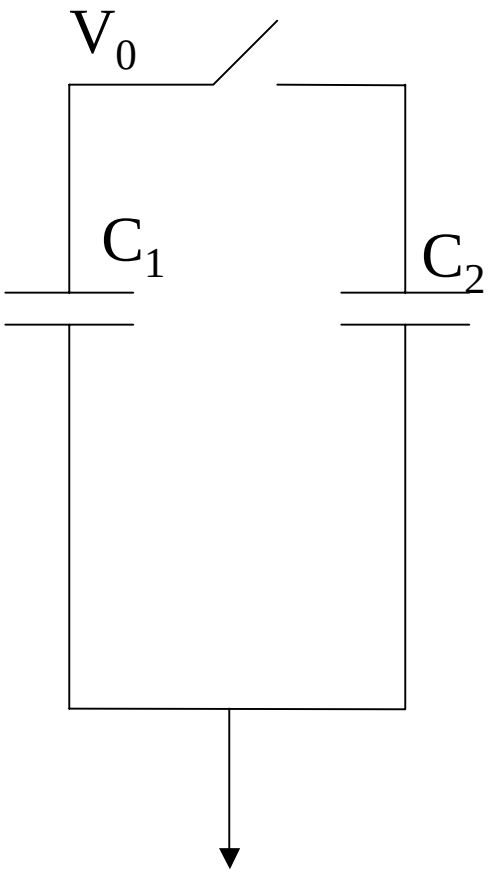
Why is this worse than resistive load?

Recharge current is only limited by available electrons!

Can cause massive voltage drop until battery catches up.

So what? Last year's capstone project: sonar firing caused processor reset

Charge Sharing



1. Initially $Q_1=V_0C_1$
2. Then close switch, what is V'/V_0 ?
3. **$V_0 = Q_1/C_1$ (initial condition)**
4. **$Q_1'+Q_2' = Q_1$ (post condition)**
5. $Q_1 = V'C_1+V'C_2 = V'(C_1+C_2)$
6. $V' = Q_1/(C_1+C_2)$
7. $V'/V0 = Q_1/(C_1+C_2) * C_1/Q_1$
8. $V'/V_0 = C_1/(C_1+C_2)$

If C_1 dominates, then $V' \sim V_0$

If $C_1 = 10C_2$ Then $V_1/V_0 = 10/11$