INTRINSYC

CerfBoard™ SA1110™

CerfBoard™ SA1110™ Hardware Design Document

ICS-HW-DD-SA1110 (part # 073-0300) Version 3.0

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About this Document

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Chapter 1 - Introduction

The purpose of this document is to describe the design of the CerfBoard, allowing developers to implement the Flash programming software, bootloader, and applications.

1.1 Intended Audience

This document is intended for development staff. This document contains the phrase “Company Confidential” at the bottom of each page and as such is to be considered proprietary to Intrinsyc Software, Inc.

1.2 Document Structure

This document is structured into the following sections:

Preface
This section contains the Cover Page, About this Document (page i), Table of Contents (begins p. ii), and Table of Figures (begins page v). Please note that all Preface pages are notated in lower-case Roman numerals.

Chapter 1 - Introduction
This section contains the Purpose of Document, the Intended Audience, the Reference Documents, and Acronym Descriptions used throughout this Document. These pages are numbered with page number notation.

Chapter 2 - CerfBoard Overview
This section provides the context for the CerfBoard.

Chapter 3 - SA-1110 Details
This section provides an explanation of the SA-1110 and its pin assignments (pin vs. BGA pad).

Chapter 4 – Break-Out Board Details
This section presents the power requirements and pinouts of the connectors on the CerfBoard.

Chapter 5 - Parts List
This section contains the CerfBoard parts list along with the cabling interconnection details.

1.3 Reference Documents

Intel™ StrongARM™ SA-1110 Microprocessor: Advanced Developer’s Manual
The fastest, easiest way to obtain a copy of the *Intel™ StrongArm™ SA1110 Microprocessor Advanced Developer’s Manual* is to download it from Intel’s website at:

http://developer.intel.com/design/strong/manuals/278240.htm

1.4 Acronyms

Acronyms used throughout this guide are listed below in alphabetical order:

Acronym:	Definition:
CPU	Central Processor Unit
GPIO	General Purpose Input/Output
IrDA	Infrared Data Association
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LED	Light Emitting Diode
PCMCIA	Personal Computer Memory Card International Association
SDRAM	Synchronous Dynamic Random Access Memory
USB	Universal Serial Bus

Chapter 2 - Overview

2.1 CerfBoard Specifications

2.1.1 Overview

The CerfBoard v3.0 integrates an Intel StrongArm 1110 microprocessor, 16 MB Flash, 32MB SDRAM, and an Ethernet adapter (see Figure 1). Three RS232 serial ports (2 line) are available through a standard dual row 10-pin header. Other interfaces include 16 digital I/O lines (all lines have programmable interrupt capability and the first four have LED indicators), LCD interface, Compact Flash socket, USB interface, and JTAG interface. The Flash memory is in-circuit programmable through the SA-1110's JTAG interface.

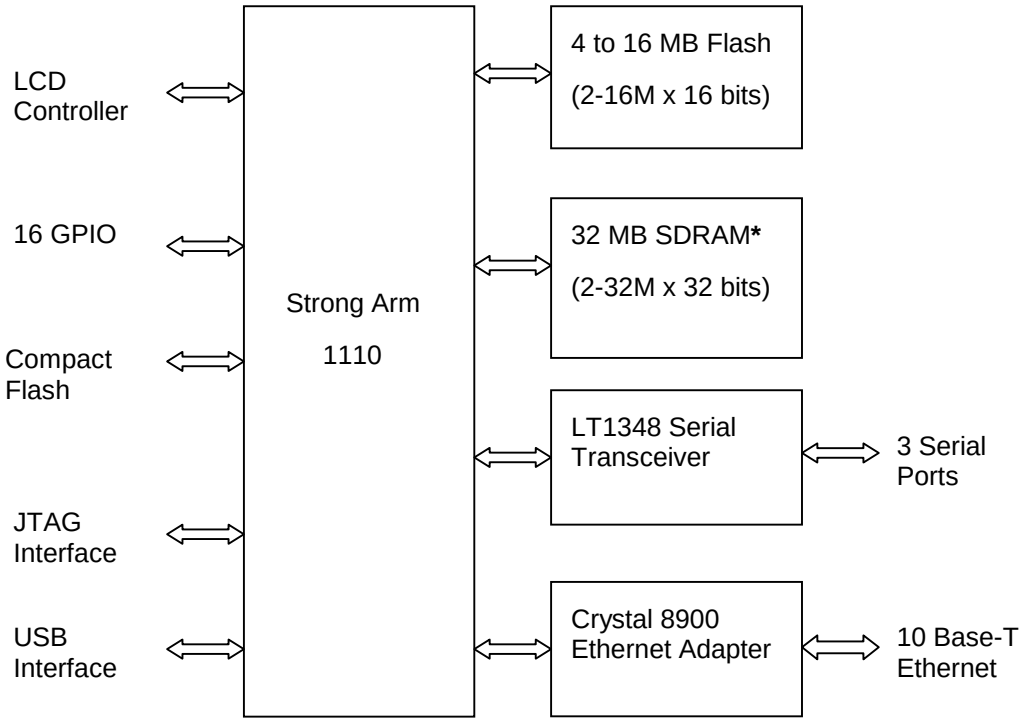

Figure 1 - CerfBoard Block Diagram

***** Other options are available. Contact Intrinsyc for details.

Note: When handling your CerfBoard SA1110, please note that the unit is an electronic device, and as such is sensitive to electrostatic discharge (ESD). Please follow ESD prevention procedures when handling the CerfBoard SA1110. After having removed your CerfBoard SA1110 from the ESD bag, place on a flat, clean, dry surface (preferably a grounded antistatic mat).

2.1.2 Features Supported

The following table defines the features supported by the standard CerfBoard and describes its hardware capacity:

Item	Description
CPU	Intel™ StrongArm™ SA1110 CPU @ 192MHz
Memory	16MB Intel StrataFlash memory using a 16-bit data bus
SDRAM	32MB SDRAM using a 32-bit data bus
Serial & I/O	3 RS232 ports, 16 digital I/O lines
Display(s)	4 LEDs
Power	5.0VDC, 1Amp Peak Power
Miscellaneous	Expansion pins–address, data bus, power and control signals
Dimensions	69mm by 57mm
Ethernet	10 Base-T
Compact Flash	Type I/II CF/CF+
USB	Type B receptacle (Device)

Figure 2 - Table of Supported CerfBoard Features

2.2 Break-Out Board Specifications

2.2.1 Overview

The CerfBoard SA1110 Break-Out Board v2.1 allows the developer to have easy access (through industry standard connectors) to the GPIO and Serial ports on the CerfBoard SA1110. In addition, the Break-Out Board has on-board LCD support to directly drive Kyocera 3.8” and 5.7” Quarter VGA displays (with touch panel). On-board DC-DC converters provide power for the LCD backlight inverter as well as LCD biasing. A general LCD header is available for driving 16 bit LCDs. Special modifications are needed to support Kyocera 7.2” VGA displays. Contact Intrinsyc for details.

2.2.2 Features Supported

The CerfBoard SA1110 Break-Out Board has the following features:

- Direct support for Kyocera 3.8” and 5.7” Quarter VGA LCDs, including touch panel interface.
- Two DC-DC converters to provide 12V for the backlight inverter, and 20-35V for the LCD contrast adjustment.
- General LCD header allows other displays to be connected to the Break-Out Board.
- Mono on-board speaker, 1/8” jack for a pair of amplified speakers.
- Mono microphone input, 1/8” jack.
- Three (3) serial ports broken out to DB9 connectors.
- Sixteen (16) GPIO lines buffered through bi-directional I/O buffers and broken out to two (2) standard 2x8 (0.1” spacing) headers. Each GPIO line can be set high or low (when configured as an input) using DIP switches. The 16 GPIO lines can be configured as 16 inputs, 16 outputs, or 8 inputs and 8 outputs.

- Four (4) Analog Inputs are exposed through a 2x5 connector. Eight (8) additional unbuffered digital I/Os are available on a 2 x 8 connector.
- JTAG input is buffered to allow 5V Corelis JTAG cards to be used with the CerfBoard SA1110.

2.2.3 Break-Out Board Block Diagram

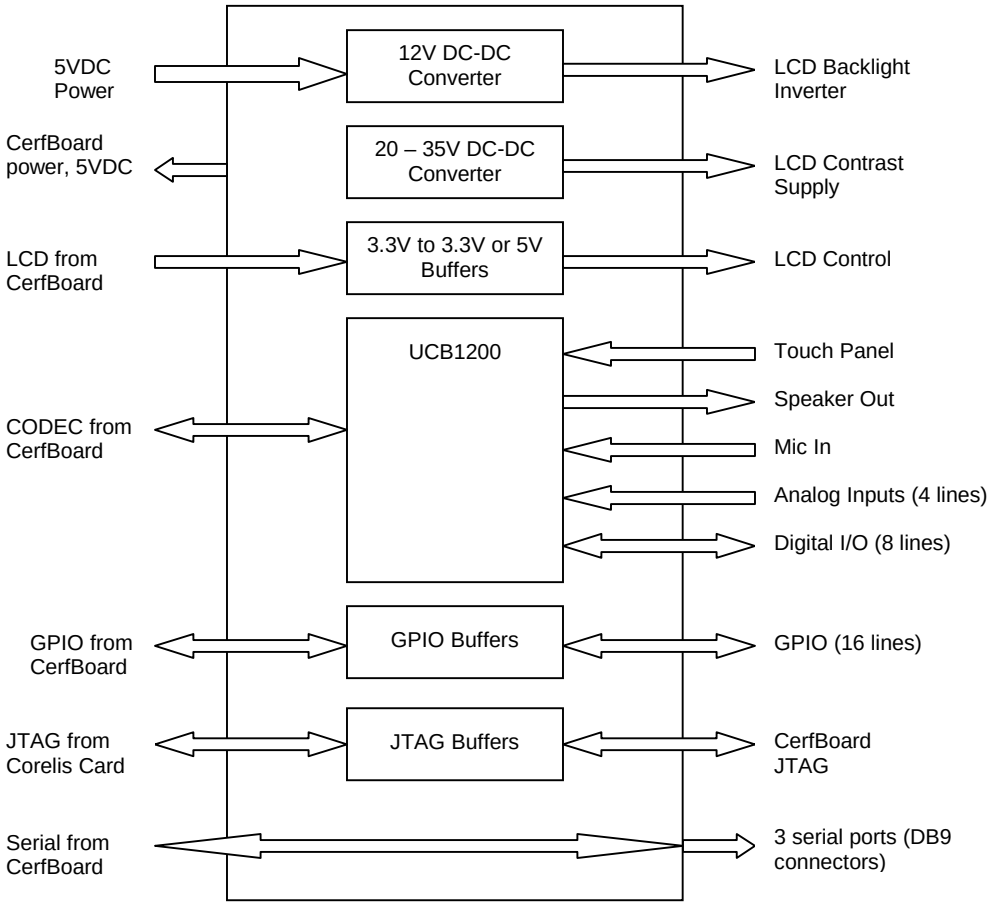

Figure 3 - Break-Out Board Block Diagram

Chapter 3 - CerfBoard SA1110 Details

3.1 SA-1110 Processor

The SA-1110 CPU was used in this design without the companion SA-1111 chip, as all the necessary functions needed for the board are included in the SA-1110.

The SA-1111 companion chip would add PS/2 ports, AC-link, I2S and L3 serial ports, an SSP data port, PWM outputs, one additional PCMCIA interface, as well as Compact Flash and GPIO interfaces.

3.1.1 SA-1110 Pin Assignments

Intel has assigned two sets of pin designators for the SA-1110: logical pin numbers from 1 to 256 are used in Intel's schematics, and physical designators A1-A16, B1-B16,…, T1-T16 are assigned to the BGA pads. There is unfortunately no correspondence between the logical pins and the physical designators (i.e. Logical pin 1 does not correspond to pad A1). The mapping from logical pin to physical pad is in Section 14 of document RF-1.

The Accel Schematic Tool used to develop the CerfBoard- SA1110 does not allow non-numerical pad designators, so for the SA-1110 the physical pads were numbered numerically: A-1 to A-16 is 1 to 16, B-1 to B17 is 17 to 32, etc. Figure 4 describes this relationship. Note that in Intrinsyc's schematics, the numerical BGA pad designators are used.

BGA PAD	Signal	Pin	BGA PAD	Signal	Pin	BGA PAD	Signal	Pin	BGA PAD	Signal	Pin
1	Vssx	4	65	D17	13	129	D13	34	193	SDCKE0	52
2	SCLK_C	224	66	D9	12	130	D20	31	194	SDCKE1	50
3	PWR_EN	222	67	D24	10	131	D28	32	195	SDCLK1	51
4	BATT_FAULT	218	68	D0	7	132	D5	33	196	Vddx2	241
5	TDI	215	69	Vssx	48	133	Vddx2	116	197	Vddx2	242
6	TCK_BYP	211	70	Vddx1	97	134	D12	30	198	GP15	73
7	Vdd	206	71	Vddx1	107	135	Vssx	244	199	Vddx1	235
8	PEXTAL	202	72	Vddx1	178	136	Vssx	245	200	GP7	83
9	Vss	199	73	Vddx1	188	137	Vssx	246	201	Vddx1	236
10	TXD_3	196	74	Vddx1	198	138	Vssx	247	202	GP3	91
11	TXD_1	192	75	Vddx1	220	139	Vssx	248	203	Vddx1	237
12	UDC-	189	76	Vddx2	3	140	Vddx2	128	204	LDD0	99
13	A3	183	77	A14	166	141	RD/~WR	143	205	~IOS16	120
14	A6	180	78	A17	163	142	~CAS0	142	206	~PREG	122
15	A7	179	79	A19	161	143	~CAS1	141	207	~PCE2	123
16	A8	176	80	A21	157	144	Vdd	140	208	~PWAIT	121
17	RXD_C	1	81	D10	18	145	D6	39	209	SDCLK0	53
18	Vssx	16	82	D2	17	146	D21	35	210	Vss	56
19	SRFM_C	223	83	D25	14	147	D29	36	211	Vdd	55
20	~TRST	217	84	D1	11	148	D14	40	212	GP24	62
21	TDO	216	85	Vddx2	238	149	Vddx2	138	213	GP18	70
22	TESTCLK	212	86	Vssx	58	150	Vssx	249	214	GP14	74
23	~RESET	207	87	Vssx	66	151	Vssx	250	215	GP10	80
24	PXTAL	203	88	Vssx	76	152	Vssx	251	216	GP8	82
25	TXTAL	200	89	Vssx	86	153	Vssx	252	217	GP5	89
26	RXD_2	193	90	Vssx	98	154	Vddx1	225	218	GP1	93

BGA PAD	Signal	Pin	BGA PAD	Signal	Pin	BGA PAD	Signal	Pin	BGA PAD	Signal	Pin
27	RXD_1	191	91	Vssx	108	155	Vddx1	226	219	L_PCLK	96
28	A2	184	92	Vddx2	15	156	Vddx2	150	220	LDD3	102
29	A5	181	93	A23	155	157	~CAS3	135	221	LDD7	106
30	A10	174	94	A20	158	158	Vss	139	222	Vss	117
31	A9	175	95	A22	156	159	~CAS2	136	223	Vdd	118
32	A12	172	96	A25	153	160	~RAS0	134	224	PSKTSL	119
33	Vdd	5	97	D19	23	161	D7	43	225	GP27	59
34	TXD_C	2	98	D3	21	162	D30	42	226	GP25	61
35	Vssx	28	99	D26	20	163	D22	41	227	GP22	64
36	VDD_FAULT	221	100	D18	19	164	D15	44	228	GP20	68
37	TCK	214	101	Vddx2	27	165	Vddx2	160	229	GP17	71
38	TMS	213	102	Vssx	115	166	Vssx	253	230	GP13	77
39	~RESET-OUT	208	103	Vssx	127	167	Vssx	254	231	GP12	78
40	Vddp	204	104	Vssx	137	168	Vssx	255	232	GP6	84
41	TEXTAL	201	105	Vssx	149	169	Vssx	256	233	Vss	88
42	RXD_3	195	106	Vssx	159	170	Vddx1	227	234	GP2	92
43	UDC+	190	107	Vssx	169	171	Vddx1	228	235	L_BIAS	95
44	A1	185	108	Vddx2	37	172	Vddx2	170	236	LDD2	101
45	A4	182	109	A24	154	173	~RAS1	133	237	LDD5	104
46	A11	173	110	~CS0	152	174	~RAS2	132	238	L_LCLK	109
47	Vdd	168	111	~CS1	151	175	~RAS3	131	239	~POE	111
48	A15	165	112	~CS2	148	176	~SDCAS	130	240	~PIOW	114
49	D16	9	113	D4	29	177	D31	46	241	GP26	60
50	D8	8	114	Vss	26	178	D23	45	242	GP23	63
51	Vss	6	115	Vdd	25	179	SDCLK2	49	243	GP21	67
52	Vssx	38	116	D27	24	180	SMROM_EN	54	244	GP19	69
53	Vddx1	65	117	Vddx2	47	181	Vddx2	239	245	GP16	72
54	ROMSEL	210	118	D11	22	182	Vddx1	229	246	GP11	79
55	Vddx3	209	119	Vssx	177	183	Vddx1	230	247	GP9	81
56	Vss	205	120	Vssx	187	184	Vddx1	231	248	Vdd	87
57	Vddx1	75	121	Vssx	197	185	Vddx1	232	249	GP4	90
58	TXD_2	194	122	Vssx	219	186	Vddx1	233	250	GP0	94
59	Vddx1	85	123	Vssx	243	187	Vddx1	234	251	LDD1	100
60	A0	186	124	Vddx2	57	188	Vddx2	240	252	LDD4	103
61	A13	171	125	RDY	144	189	~WE	125	253	LDD6	105
62	Vss	167	126	~CS3	147	190	~SDRAS	129	254	L_FCLK	110
63	A16	164	127	~CS4	146	191	~OE	126	255	~PWE	112
64	A18	162	128	~CS5	145	192	~PCE1	124	256	~PIOR	113

Figure 4 - Table of Numerical BGA vs. Pin Designators

3.1.2 Serial Debug Port

Any of the three RS-232 ports on the Serial1 connector can be used as the serial debug port (see later this chapter for pinout). The software that ships with the CerfBoard uses Serial Port 3 as the debug port. All three ports use the LT1348 transceiver to convert the SA-1110's 3V signals to RS-232 levels and vice-versa. The LT1348 has separate enable pins for its receivers and transmitters and these are controlled by GPIO25 (transmitters) and GPIO24 (receivers) on the SA-1110. GP25 and GP24 must be programmed as outputs and be driven high to enable the LT1348. This must be done before any debug messages are sent or received (if one of the serial ports is used as a debug port).

3.2 Power Supply and I/O Specification

3.2.1 Parts Placement Diagram

A simplified CerfBoard Parts Placement Diagram is show in Figures 5 and 6. Pin 1 for all the dual-row headers is indicated by a “1” in the diagram.

3.2.2 J1: Power Connector

The power connector is a standard 1.1mm barrel connector (CUI Stack PJ-007). The power supply specifications are as follows:

- Voltage: 5 V Regulated, +/- 5%, center negative.
- Current: 500 mA if the CerfBoard is used without any Compact Flash cards. Under normal operating conditions, the CerfBoard will draw an average of 300 mA (preliminary specification). Compact Flash cards can draw peak currents of 500 mA, thus a supply with a 1.0 A capacity should be used if a Compact Flash card such as an IBM MicroDrive is used.

Note: THE *CerfBoard* REQUIRES A REGULATED 5V SUPPLY. A STANDARD UNREGULATED PLUG-IN WALL TRANSFORMER RATED AT 5V AND 500 mA WILL NOT WORK AND WILL DAMAGE THE BOARD.

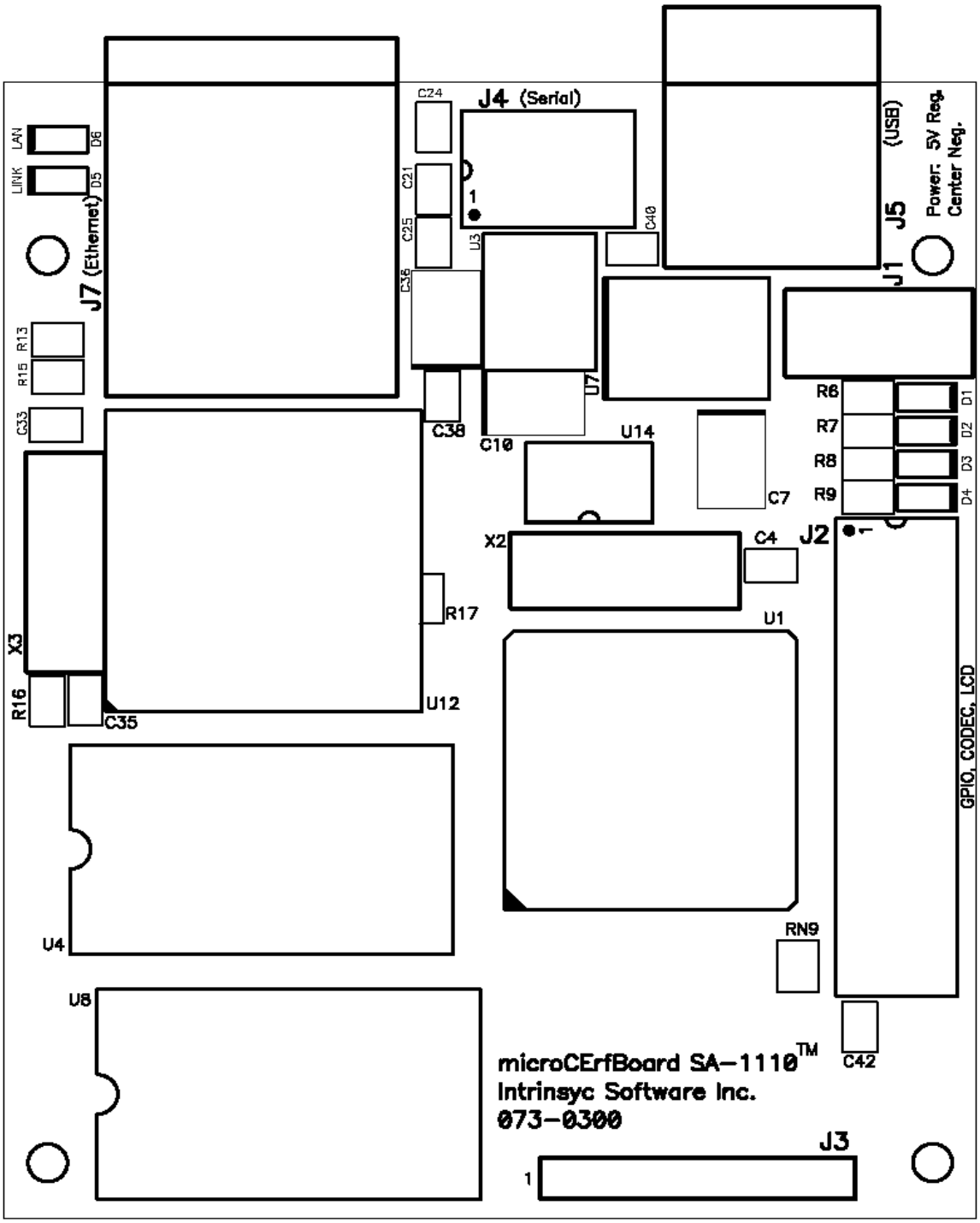

Figure 5 - CerfBoard Top Side Parts Placement Diagram

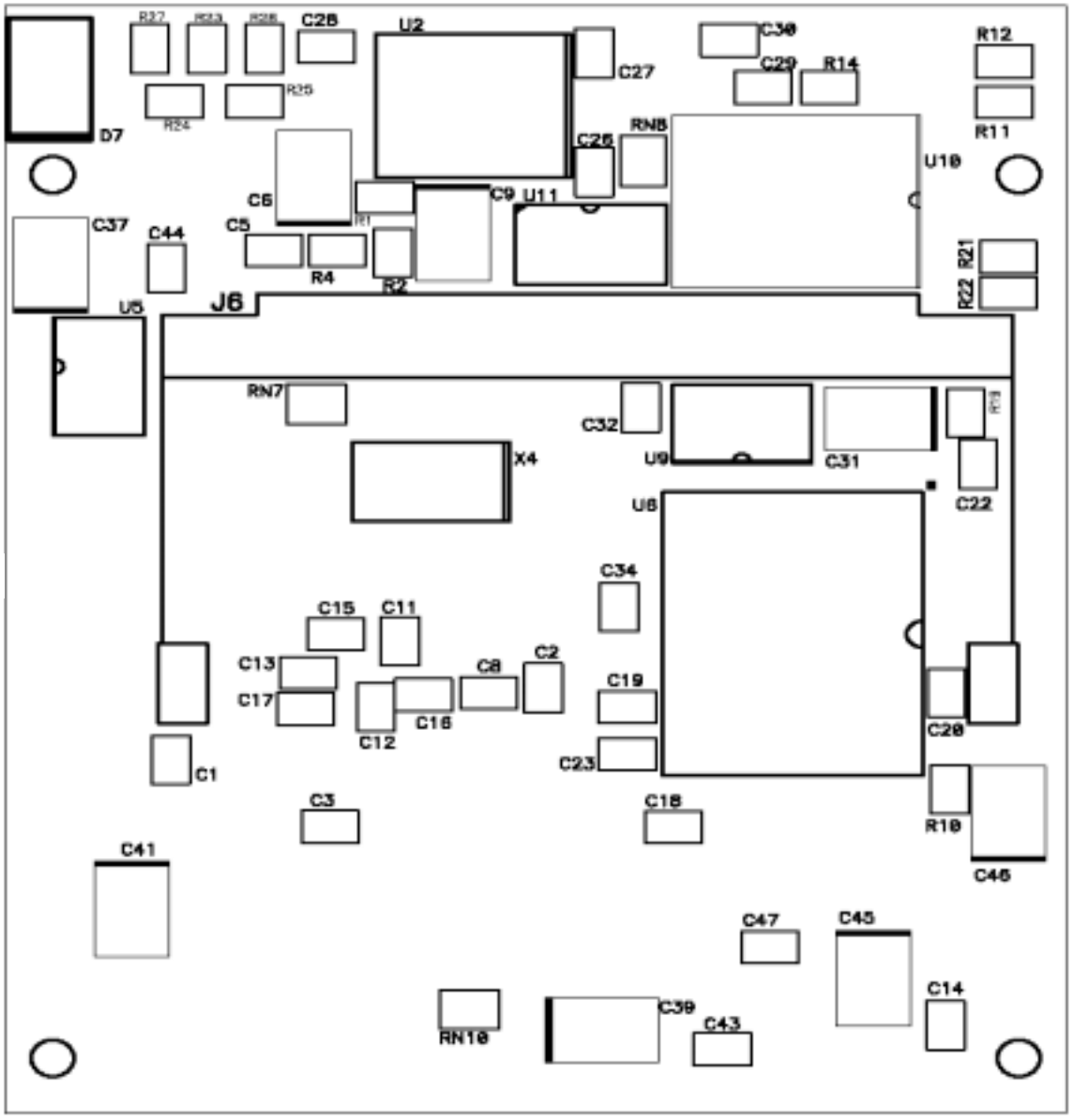

Figure 6 - CerfBoard Bottom Side Parts Placement Diagram

3.2.3 J2: GPIO/ LCD/CODEC Connector

The pinout of the J2 Connector (a high-density dual-row connector) is shown in Figure 7.

J2 Header Pin	Signal	J2 Header Pin	Signal
1	L_FCLK (LCD)	21	GPIO-7
2	L_LCLK (LCD)	22	GPIO-8
3	LDD0 (LCD)	23	GPIO-9
4	LDD1 (LCD)	24	GPIO-10
5	LDD2 (LCD)	25	GPIO-11
6	LDD3 (LCD)	26	GPIO-12
7	LDD4 (LCD)	27	GPIO-13
8	LDD5 (LCD)	28	GPIO-14
9	LDD6 (LCD)	29	GPIO-15
10	LDD7 (LCD)	30	GND
11	L_PCLK (LCD)	31	SCLK_C (CODEC)
12	L_BIAS (LCD)	32	SRFM_C (CODEC)
13	GND	33	RXD_C (CODEC)
14	GPIO-0 (LED)	34	TXD_C (CODEC)
15	GPIO-1 (LED)	35	GND
16	GPIO-2 (LED)	36	BATT_FAULT
17	GPIO-3 (LED)	37	VDD_FAULT
18	GPIO-4	38	nRESET
19	GPIO-5	39	UCB_IRQ
20	GPIO-6	40	GND

Figure 7 - J2 Header Pinout

Notes:

- GPIO pins GPIO-0 to GPIO-3 have active-high LED indicators (D1 to D4 in Figure 5).
- Some LCD displays require GPIO-2 to GPIO-9 in addition to the standard LCD signals.
- BATT_FAULT and VDD_FAULT are used to indicate impending battery or supply failures (active high).
- nRESET is active low hardware reset for the board. It has a 10k pull-up on board, and can be driven low for a minimum of 150 ms to reset the board, or can be used as an active low reset input by external circuitry.
- UCB_IRQ is dedicated for use with the UCB1200 on the BOB by the software.

3.2.4 J3: JTAG Connector

The pinout of the JTAG connector (a standard single-row 7-pin connector) is shown in Figure 8. See Section 3.6 for details on programming the Flash through the JTAG interface.

JTAG Header Pin	JTAG Signal
1	TMS
2	TDI
3	TDO
4	TCK
5	nTRST
6	GND
7	+3.3 V Out

Figure 8 - J3 Pinout

Note: Pin 7 provides +3.3 V to power external level conversion circuitry if required (25 mA max).

3.2.5 J4: Serial Connector

The pinout of the Serial Connector (a high-density dual-row connector) is shown in Figure 9.

Serial Connector Header Pin	Signal
1	S1_RX (RS232)
2	S1_TX (RS232)
3	GND
4	GND
5	S2_RX (RS232)
6	S2_TX (RS232)
7	+3.3V Out
8	GND
9	S3_RX (RS232)
10	S3_TX (RS232)

Figure 9 - Serial Header Pinout

Note: Pin 7 provides +3.3V to power an external IRDA transceiver board (serial Port 2 can be used as an IRDA transceiver). The transceiver board should draw no more than 25 mA. Because Serial Port 2 is

RS-232 compatible, an RS-232 transceiver will have to be used on the IRDA transceiver board to interface to the CerfBoard board.

3.2.6 J5: USB Connector

The pinout of the USB Connector (a standard Type B USB connector) is shown in Figure 10:

USB Connector Header Pin	Signal
1	Vbus (Not Connected)
2	D-
3	D+
4	GND
5	Shield (GND)
6	Shield (GND)

Figure 10 - USB Connector Pinout

3.2.7 J6: Compact Flash Connector

The pinout of the J6 Connector (TYPE II CF+ connector) is shown in Figure11:

J6 Header Pin	Signal	J6 Header Pin	Signal
1	GND	27	D11
2	D3	28	D12
3	D4	29	D13
4	D5	30	D14
5	D6	31	D15
6	D7	32	nPCE2
7	nPCE1	33	VS1 (Not Connected)
8	A10	34	nPIOR
9	nPOE	35	nPIOW
10	A9	36	nPWE
11	A8	37	RDY/nBUSY
12	A7	38	Vcc In (3.3V)
13	Vcc In (3.3V)	39	nMASTER
14	A6	40	VS2 (Not Connected)
15	A5	41	RESET
16	A4	42	nWAIT
17	A3	43	NINPACK (Not Connected)
18	A2	44	NPREG
19	A1	45	BVD1
20	A0	46	BVD2
21	D0	47	D8
22	D1	48	D9
23	D2	49	D10
24	nIOIS16	50	GND
25	nCD1	51	ESD Clip (GND)
26	nCD2	52	ESD Clip (GND)

Figure 11 - J6 CF Header Pinout

Notes:

- Signals that start with an “n” are active low.
- Compact Flash (CF) cards are NOT hot-swappable in this design – power must be removed from the board before the card is swapped out. The reason for this is that tri-state buffers for address and data were not used to keep the board size small.
- Only 3.3V CF cards are supported.
- A CF Type II header is used to allow Type I or II CF (or CF+) cards to be used.
- Several GPIO pins are used to interface to the CF card (these GPIO pins are not exposed on the J2: GPIO Connector) in addition to the data, address, and PCMCIA pins. These pins are:

  Reset: This pin is connected to GPIO 21. The reset polarity depends on the type of CF card: active high for memory and I/O mode, active low for IDE mode.

  RDY/nBSY: This pin is connected to GPIO 22.

  nCDx: These pins are connected through an OR gate (same as a negative logic AND gate) to GPIO 23. A low signal on GPIO 23 indicates that the CF card has been inserted into the CF header.

  BVDx: These pins are connected to GPIO pins 19 and 20. They are special purpose pins (functions vary with memory, I/O, and IDE modes).
- The following CF pins have the following connections:

  nCSEL is connected to GND to indicate to the CF device in IDE mode to configure itself as a Master. This pin is not used in Memory or I/O modes.

  VS1 and VS2: these pins are unconnected because only 3.3V CF cards are supported.

  nINPACK: this pin is an output from the CF card that enables tri-state buffers connected to the data bus. Since tri-state buffers are not used in this design, this pin is unconnected.

3.2.8 J7: Ethernet Connector

The pinout of the J7 Connector (a standard RJ45 connector) is shown in Figure 12:

RJ45 Pin	Signal
1	TXD+
2	TXD-
3	RXD+
4	NC
5	NC
6	RXD-
7	NC
8	NC
9	NC (Mounting Hole)
10	NC (Mounting Hole)
11	Shield (GND)
12	Shield (GND)

Figure 12 - J7 Pinout

3.3 Memory Organization

3.3.1 SDRAM

The SDRAM consists of two 128MBit devices organized as 8MWords x 32 bits. The Chip Select pin (nCS) is connected to nRAS0/nSDCS0 (pad 160) on the CPU. Other connections from the CPU to the SDRAM are as recommended in the SA-1110 manual. The SDRAM's base address is 0xC0000000.

SDRAM memory	Reserved for power handlers	0C000000
		0C000FFF
SDRAM memory	BCEDDK Memory Pool	0C001000
		0C01FFFF
SDRAM memory	Reserved for Driver Global	0C020000
		0C020FFF
SDRAM memory	Reserved for Ethernet Debugging	0C021000
		0C040FFF
SDRAM memory	Reserved for power handlers	0C058000
		0C058FFF
SDRAM memory	Reserved for RAM	0C100000
		0C7FFFFE

Figure 13 - SDRAM Memory Map

3.3.2 Flash Memory

The Flash memory is a single-chip Intel E28FxxxJ5 or E28FxxxJ3 (TSOP package) Flash device organized as 2, 4, or 8 MWords x 16 Bits. The Chip Select pin (CE0) is connected to nCS0 (pad 110) on the CPU. Thus the base address of the Flash is: 0x0000000. After reset, the SA-1110 will start executing instructions in the Flash starting at 0x0000000. The ROM_SEL pin on the SA-1110 has been tied Low to enable 16-bit memory at 0x0000000.

Flash memory	Bootloader	00000000
		0001FFFF
Flash memory	Reserved Area	00020000
		0003FFFF
Flash memory	Windows CE image	00040000
		0023FFFF
Flash memory	Optional Flash file system or larger Windows CE image	00240000
		003FFFFF

Figure 14 - Flash Memory Map

3.4 Ethernet Adapter

A Crystal 8900A is used as the Ethernet adapter. The 93L66 EEPROM is used to store configuration information. A standard shielded RJ45 is used – see section 3 for the pinout. LED D5 indicates if Link pulses are present and LED D6 indicates LAN activity (see Figure 5).

3.4.1 Interface to SA-1110

The SA-1110 does not have an ISA bus interface, so a simple interface was implemented using the nCS1 (pad 111) of the CPU and the RD/nWR line. The interface supports I/O mode only. The base address of the 8900 is 0x08000000.

The interrupt line from the 8900A, INTRQ0, is connected to GP26 (GPIO 26) on the SA-1110. This SA-1110 input must be programmed to generate an active high interrupt for this line to be used for the 8900A interrupts.

3.5 Low-Power Management

The CerfBoard supports the following low-power management features for CPU Sleep mode:

- Core voltage supply disable: during sleep, the SA-1110 has the ability to disable the core supply, saving power. This feature is supported through the use of the PWR_EN pin, which is used to enable the core supply regulator only when the CPU is not in sleep mode. The 1.8 V regulator consumes 1 uA during shutdown.
- The Flash consumes less than 100 uA in sleep mode if the nRP pin is brought low. If nRP is allowed to stay high the current consumption may be as high as 1 mA. The Flash nPR pin is thus connected to nRESET_OUT from the CPU, which is brought low during CPU Sleep mode.
- The RS-232 Transceiver can be turned off using the GPIO pins 25 and 24. Power consumption during shutdown is less than 1 uA.
- SDRAM: the CPU supports holding the SDRAM in self-refresh mode during CPU Sleep mode. Current consumption during self-refresh is 4 mA maximum.
- Ethernet: The 8900a can be placed into hardware sleep mode by setting bit 9 of the 8900a's SelfCTL register and asserting the nHWSLEEP pin. This pin is connected to GPIO 27. The 8900a should only be placed in sleep mode if an interrupt from the 8900a is not expected to wake up the CPU. Power consumption is 100 uA during sleep mode.
- The 3.3V regulator has a quiescent current of 85 uA.

The CPU consumes a maximum of 75 uA during Sleep mode, so the total current consumption during sleep mode should be less than 4.5 mA. However, this value has not been fully qualified.

3.6 Flash JTAG Programming

In-circuit programming of the Flash for the bootloader is done through the CPU's JTAG interface, rather than using a CPLD.

3.6.1 Flash Pin Assignments

The Flash pin assignments are contained in Figure 15:

Flash Pin (TSSOP)	Flash Pin Definition	SA 1110 Pad	Flash Pin (TSSOP)	Flash Pin Definition	SA 1110 Pad
1	A22	95	29	CE2	-
2	CE1	-	30	A23	93
3	A21	80	31	BYTE#	-
4	A20	94	32	A0	60
5	A19	79	33	D0	68
6	A18	64	34	D8	50
7	A17	78	35	D1	84
8	A16	63	36	D9	66
9	Vcc	-	37	Vcc	-
10	A15	48	38	D2	82
11	A14	77	39	D10	81
12	A13	61	40	D3	98
13	A12	32	41	D11	118
14	CE0	110	42	GND	-
15	Vpen	-	43	Vccq	-
16	RP#	39	44	D4	113
17	A11	46	45	D12	134
18	A10	30	46	D5	132
19	A9	31	47	D13	129
20	A8	16	48	GND	-
21	GND	-	49	D6	145
22	A7	15	50	D14	148
23	A6	14	51	D7	161
24	A5	29	52	D15	164
25	A4	45	53	STS	-
26	A3	13	54	OE#	191
27	A2	28	55	WE#	189
28	A1	44	56	A24	109

Figure 15 - Flash Pin Assignments for JTAG Programming

The following notes need to be considered when modifying Flash programming software for the new CerfBoard:

- The STS pin cannot be read.
- The BYTE# is permanently held High to enable 16 bit mode only. Programming in 8-bit mode is not permitted.

3.6.2 SA-1110 Boundary Scan Mode

The SA-1110 can be placed into Boundary Scan Mode by driving the nTRST pin low and then high. This pin is available on the JTAG header as pin 5. Pin 7 supplies +3.3V to power any level conversion/clamp circuitry that may be required when connecting to a JTAG card. The absolute maximum level on any input line is +3.6 V.

JTAG Header Pin	JTAG Signal
1	TMS
2	TDI
3	TDO
4	TCK
5	nTRST
6	GND
7	+3.3V

Figure 16 - JTAG Header Pin Assignments

Chapter 4 - Break-Out Board Details

4.1 Parts Placement Diagram

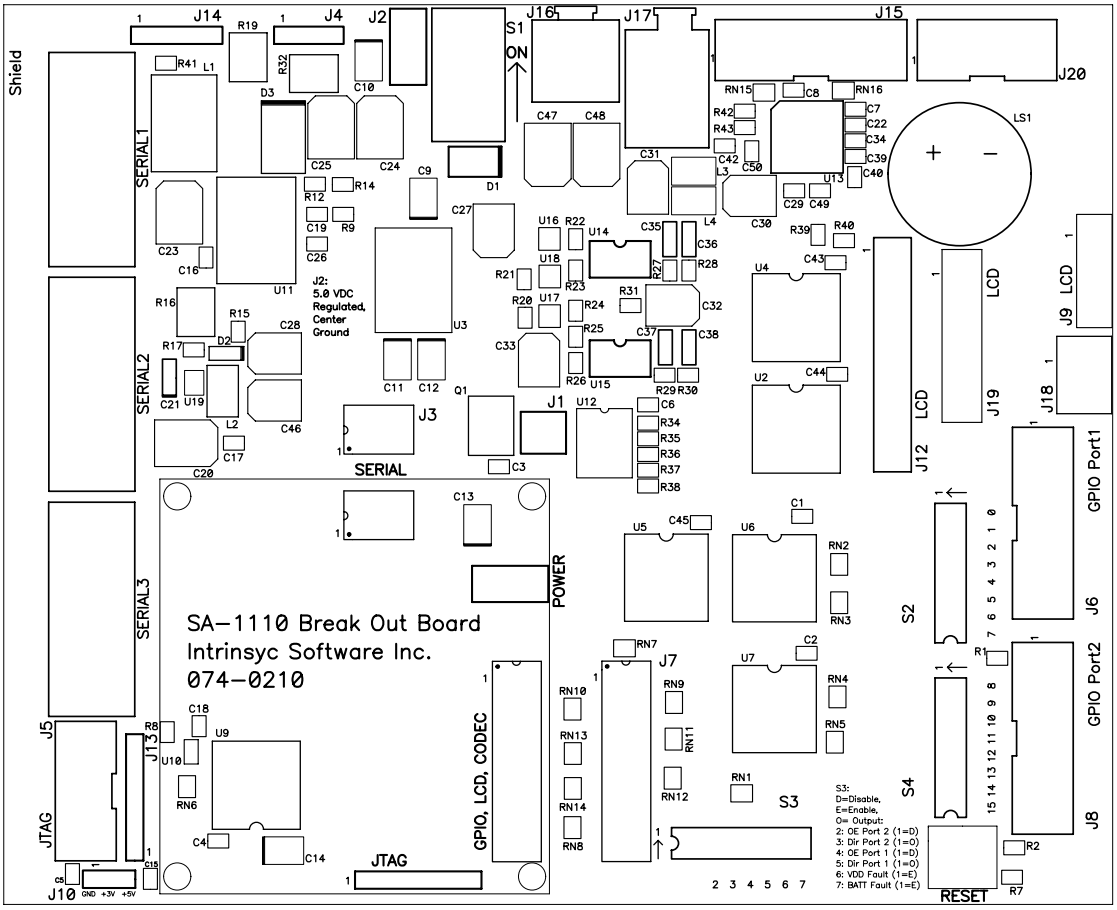

Figure 17 - Break-Out Board Parts Placement Diagram

4.2 Power Supply and I/O Specification

4.2.1 Power Supply

The wall-mount power supplied with the CerfBoard SA1110 will work with the Break-Out Board. The power supply is a CUI Stack Model DPS050280U-P7 (with inverted connector), which supplies a regulated 5V DC output at up to 2.4 Amps. Power Supply requirements of the Break-Out Board are as follows:

- Voltage:

  5 V Regulated, +/- 5%, center negative.

- Current:

  500mA no display, no Compact Flash cards
  Add 500mA for Compact Flash
  Add 800mA for 5.7" Kyocera High-Brightness LCD Backlight

- Total Requirement:

  1.8A at 5VDC.

Note: DO NOT USE AN UNREGULATED POWER SUPPLY FOR THE BREAK-OUT BOARD. DOING SO WILL PERMANENTLY DAMAGE THE BREAK-OUT BOARD AND THE CERFBOARD SA1110.

4.2.2 I/O Specification

The following table provides an overview of the connectors on the Break-Out Board. The following subsections provide detailed specifications on each connector.

Connector	Function
J1	Power for CerfBoard SA1110 board.
J2	Input power from wall-mount power supply.
J3	Serial connector to CerfBoard SA1110 board.
J4	Power Connector for D12M60J type LCD Backlight Inverter.
J5	JTAG connector to Corelis JTAG card.
J6	GPIO connector for GPIO-0 to GPIO-7.
J7	40 Pin Connector to CerfBoard SA1110 board (GPIO, LCD, CODEC).
J8	GPIO connector for GPIO-8 to GPIO-15.
J9	LCD connector for 22-pin FPC cable for 3.8” Kyocera LCDs.
J10	Power out connector to power off-board circuitry.
J11	Not used.
J12	General-purpose 2x13 header for LCD displays.
J13	JTAG connector to CerfBoard SA1110.
J14	Power Connector for PH-BLC08-K3 type LCD Backlight Inverter.
J15	UCB 1200 digital I/O connector.
J16	Audio out.
J17	Microphone in.
J18	4-wire resistive touch screen input connector.
J19	LCD connector for 15-pin cable for 5.7” Kyocera LCDs.
J20	UCB 1200 Analog Input connector.
Serial 1	Serial Port 1 from SA-1110.
Serial 2	Serial Port 2 from SA-1110.
Serial 3	Serial Port 3 from SA-1110 (debug port).

Figure 18 - Connector Definitions

4.2.3 J1: CerfBoard SA1110 Power Connector

The power connector is a standard 1.1mm barrel connector (MLSS100-2-D).

Note: THE *CerfBoard* SA1110 REQUIRES A REGULATED 5V SUPPLY.

4.2.4 J2: Input Power Jack

The input power jack is of type CUI Stack PJ-007.

Note: THE INPUT POWER JACK CONNECTOR IS CENTER GROUND.

4.2.5 J3: Serial connector to CerfBoard

The pinout of the Serial Connector (a high-density dual-row connector) is shown in Figure 19.

J3 Header Pin	Signal
1	S1_RX (RS232)
2	S1_TX (RS232)
3	GND
4	GND
5	S2_RX (RS232)
6	S2_TX (RS232)
7	Not Connected
8	GND
9	S3_RX (RS232)
10	S3_TX (RS232)

Figure 19 - J3 Header Pinout

4.2.6 J4: Power Connector for LCD Backlight Inverter

The pinout of the Power Connector for the LCD Backlight Inverter of type D12M60J (Endicott) or equivalent is shown in Figure 20:

J4 Header Pin	Signal
1	+12V
2	GND
3	Brightness Adjustment
4	Not connected

Figure 20 - J4 Header Pinout

4.2.7 J5: JTAG Connector to Corelis JTAG Card

The pinout of the JTAG Connector to Corelis JTAG Card is shown in Figure 21:

J5 Header Pin	Signal
1	nTRST
2	GND
3	TDO
4	GND
5	TDI
6	GND
7	TMS
8	GND
9	TCK
10	GND

Figure 21 - J5 Header Pinout

4.2.8 J6: GPIO Connector for GPIO-0 to GPIO-7

The pinout of the GPIO Connector for GPIO-0 to GPIO-7 is shown in Figure 22:

J6 Header Pin	Signal
1	GPIO-0
2	GND
3	GPIO-1
4	GND
5	GPIO-2
6	GND
7	GPIO-3
8	GND
9	GPIO-4
10	GND
11	GPIO-5
12	GND
13	GPIO-6
14	GND
15	GPIO-7
16	GND

Figure 22 - J6 Header Pinout

4.2.9 J7: GPIO/ LCD/CODEC Connector

The pinout of the J7 Connector (a high-density dual-row connector) is shown in Figure 23:

J7 Header Pin	Signal	J7 Header Pin	Signal
1	L_FCLK (LCD)	21	GPIO-7
2	L_LCLK (LCD)	22	GPIO-8
3	LDD0 (LCD)	23	GPIO-9
4	LDD1 (LCD)	24	GPIO-10
5	LDD2 (LCD)	25	GPIO-11
6	LDD3 (LCD)	26	GPIO-12
7	LDD4 (LCD)	27	GPIO-13
8	LDD5 (LCD)	28	GPIO-14
9	LDD6 (LCD)	29	GPIO-15
10	LDD7 (LCD)	30	GND
11	L_PCLK (LCD)	31	SCLK_C (CODEC)
12	L_BIAS (LCD)	32	SRFM_C (CODEC)
13	GND	33	RXD_C (CODEC)
14	GPIO-0 (LED)	34	TXD_C (CODEC)
15	GPIO-1 (LED)	35	GND
16	GPIO-2 (LED)	36	BATT_FAULT
17	GPIO-3 (LED)	37	VDD_FAULT
18	GPIO-4	38	nRESET
19	GPIO-5	39	UCB_IRQ
20	GPIO-6	40	GND

Figure 23 - J7 Header Pinout

Notes:

- GPIO pins GPIO-0 to GPIO-3 have active-high LED indicators on the CerfBoard.
- Some LCD displays require GPIO-2 to GPIO-9 in addition to the standard LCD signals.
- BATT_FAULT and VDD_FAULT are used to indicate impending battery or supply failures (active high) (for CerfBoard only).
- nRESET is active low hardware reset for the board. It has a 10k pull-up on board, and is connected to RESET1 to allow the board (Break-Out Board and CerfBoard) to be reset.

4.2.10 J8: GPIO Connector for GPIO-8 to GPIO-15

The pinout of the GPIO Connector for GPIO-8 to GPIO-15 is shown in Figure 24:

J8 Header Pin	Signal
1	GPIO-8
2	GND
3	GPIO-9
4	GND
5	GPIO-10
6	GND
7	GPIO-11
8	GND
9	GPIO-12
10	GND
11	GPIO-13
12	GND
13	GPIO-14
14	GND
15	GPIO-15
16	GND

Figure 24 - J8 Header Pinout

4.2.11 J9: LCD Connector for 22-pin Cable for 3.8” Kyocera LCDs

The pinout of the LCD Connector for the 22-pin FPC Cable for 3.8” Kyocera LCDs is shown in Figure 25:

J9 Header Pin	Signal
1	L_FCLK
2	L_LCLK
3	L_PCLK
4	LCD_RESET
5	+3V
6	+3V
7	GND
8	DF
9	V0
10	V1
11	V2
12	V3
13	V4
14	GND
15	LDD7
16	LDD6
17	LDD5
18	LDD4
19	LDD3
20	LDD2
21	LDD1
22	LDD0

Figure 25 - J9 Header Pinout

Note: Pins 1-3 and 15-22 are buffered on the Break-Out Board. V0-V4 are bias pins which are supported on the BOB.

4.2.12 J10: Power Out Connector to Power Off-Board Circuitry

The pinout of the Power Out Connector to Power Off-Board Circuitry is shown in Figure 26:

J10 Header Pin	Signal
1	+5V
2	+3.3V
3	GND

Figure 26 - J10 Header Pinout

4.2.13 J12: General Purpose header for LCD Displays

The pinout of the General Purpose header for LCD Displays is shown in Figure 27:

J12 Header Pin	Signal
1	L_FLCK
2	L_LCLK
3	L_PLCK
4	LCD_RESET
5	LCD_PWR
6	GND
7	LCD_VEE
8	LDD15
9	LDD14
10	LDD13
11	LDD12
12	LDD11
13	LDD10
14	LDD9
15	LDD8
16	LDD7
17	LDD6
18	LDD5
19	LDD4
20	LDD3
21	LDD2
22	LDD1
23	LDD0
24	L_BIAS
25	GND
26	GND

Figure 27 - J12 Header Pinout

Note: Pins 1-4 and 8-24 are buffered on the Break-Out Board. LCD_VEE is a 20-35V DC bias pin. LCD_PWR is set by R39 or R40 on the Break-Out Board, and is 5V or 3.3V respectively.

4.2.14 J13: JTAG Connector to CerfBoard SA1110

The pinout of the JTAG Connector to CerfBoard SA1110 is shown in Figure 28:

J13 Header Pin	Signal
1	TMS
2	TDI
3	TDO
4	TCK
5	nTRST
6	GND
7	Not Connected

Figure 28 - J13 Header Pinout

4.2.15 J14: Power Connector for LCD Backlight Inverter

The pinout of the Power Connector to PH-BLC08-K3 (Hitachi) Type LCD Backlight Inverter is shown in Figure 29:

J14 Header Pin	Signal
1	+12V
2	GND
3	Backlight Enable
4	Backlight Adjustment
5	Backlight Adjustment

Figure 29 - J14 Header Pinout

4.2.16 J15: UCB 1200 Digital I/O Connector

The pinout of the UCB 1200 GPIO Connector is shown in Figure 30:

J15 Header Pin	Signal
1	UCB_IO-7
2	GND
3	UCB_IO-6
4	GND
5	UCB_IO-5
6	GND
7	UCB_IO-4
8	GND
9	UCB_IO-3
10	GND
11	UCB_IO-2
12	GND
13	UCB_IO-1
14	GND
15	UCB_IO-0
16	GND

Figure 30 - J15 Header Pinout

4.2.17 J16: Audio Out

The pinout of the Audio Out is shown in Figure 31:

J16 Header Pin	Signal
1	Analog GND
2	Audio Out
3	Not Connected
4	Not Connected
5	Audio Out

Figure 31 - J16 Header Pinout

4.2.18 J17: Microphone In

The pinout of the Microphone In is shown in Figure 32:

J17 Header Pin	Signal
1	Analog GND
2	Audio In
3	Not Connected

Figure 32 - J17 Header Pinout

4.2.19 J18: 4-Wire Resistive Touch Screen Input Connector

The pinout of the 4-Wire Resistive Touch Screen Input Connector is shown in Figure 33:

J18 Header Pin	Signal
1	TSPY
2	TSMX
3	TSMY
4	TSPX

Figure 33 - J18 Header Pinout

4.2.20 J19: LCD Connector for 5.7" Kyocera LCDs

The pinout of the LCD Connector for the 15-Pin Cable for 5.7" Kyocera LCDs is shown in Figure 34:

J19 Header Pin	Signal
1	L_FCLK
2	L_LCLK
3	L_PCLK
4	LCD_RESET
5	LCD_PWR
6	GND
7	LCD_VEE
8	LDD7
9	LDD6
10	LDD5
11	LDD4
12	LDD3
13	LDD2
14	LDD1
15	LDD0

Figure 34 - J19 Header Pinout

Note: Pins 1-4 and 8-15 are buffered on the Break-Out Board. LCD_VEE is a 20-35V DC bias pin. LCD_PWR is set by R39 or R40 on the Break-Out Board, and is 5V or 3.3V respectively.

4.2.21 J20: UCD 1200 Analog Input Connector

The pinout of the UCD 1200 Analog Input Connector is shown in Figure 35:

J20 Header Pin	Signal
1	AD3
2	Analog GND
3	AD2
4	Analog GND
5	AD1
6	Analog GND
7	AD0
8	Analog GND
9	ADCSYNC
10	GND

Figure 35 - J20 Header Pinout

Note: Nominal full-scale voltage is 7.5V. Absolute maximum voltage is 8.5V.

4.2.22 Serial 1: Serial Port 1 from the CerfBoard SA1110

The pinout of Serial Port 1 from the CerfBoard SA1110 is shown in Figure 36:

Serial 1 Header Pin	Signal
1	Not connected
2	RX
3	TX
4	Not connected
5	GND
6	Not connected
7	Not connected
8	Not connected
9	Not connected

Figure 36 - Serial 1 Header Pinout

4.2.23 Serial 2: Serial Port 2 from the CerfBoard SA1110

The pinout of Serial Port 2 from the CerfBoard SA1110 is shown in Figure 37:

Serial 2 Header Pin	Signal
1	Not connected
2	RX
3	TX
4	Not connected
5	GND
6	Not connected
7	Not connected
8	Not connected
9	Not connected

Figure 37 - Serial 2 Header Pinout

4.2.24 Serial 3: Serial Port 3 from the CerfBoard SA1110

The pinout of Serial Port 3 from the CerfBoard SA1110 is shown in Figure 38:

Serial 3 Header Pin	Signal
1	Not connected
2	RX
3	TX
4	Not connected
5	GND
6	Not connected
7	Not connected
8	Not connected
9	Not connected

Figure 38 - Serial 3 Header Pinout

4.3 Usage Instructions

4.3.1 Population Options

Your Break-Out Board was populated to accommodate either a 3.8" Kyocera LCD (3.3V I/O), a 5.7" Kyocera LCD (5V I/O), or a 7.2" Kyocera LCD (3.3V I/O). The parts population options are as follows:

Note: DO NOT USE A 3.8" LCD ON A BOARD POPULATED FOR A 5.7" LCD! DOING SO WILL PERMANENTLY DAMAGE THE LCD.

4.3.2 3.8" Kyocera QVGA Display (3.3V I/O)

Component	Value
R39	**Unpopulated**
R40	0 Ohms
U2, U4, U5	74VHC244M **(No "T")**
R15	**21K**
R34, R35, R36, R37, R38	Default Population only R38

Figure 39 - 3.8" Kyocera Display (3.3V I/O) Population Option

4.3.3 5.7" Kyocera QVGA Display (5V I/O)

Component	Value
R39	0 Ohms
R40	**Unpopulated**
U2, U4, U5	74VHCT244M **(Note the "T")**
R15	**16K**
R34, R35, R36, R37, R38	Default Population only R36

Figure 40 - 5.7" Kyocera Display (5V I/O) Population Option

Note: It is possible to leave U5, U12, U14, U15, U16, U17, U18, R20-R31, R34-R38, C32, C33, and C35-C38 unpopulated, but it is best to populate these parts to allow an easy switchover to 3.8" or 16-bit displays simply by changing U2, U4, U5, R39, R40, and R17.

4.3.4 7.2” Kyocera VGA Display (3.3V I/O)

There are a number of modifications that have to be done to support 7.2" LCDs. D2, L2, U19, C20, and C21 must be removed and modifications to R15, R16, R17, C28, C46, and C27 done to provide 1.35V to 2.55V VEE for 7.2" display.

Repopulate as follows:

Component	Value
R15	2.8K
R16	5K pot
R17	5K
C28, C46, C27	0.1 uF
R39	**unpopulated**
R40	0 ohms
U2, U4, U5	74VCH244M
R15	**2.8K**
R34, R35, R36, R37, R38	Default Population only R36

Figure 41 - Repopulation for Kyocera 7.2” Display

Note: A custom hand-assembled cable is currently needed to connect to the 7.2" display. Intrinsyc suggests making a small PCB that plugs into the main connector and provides a 1-1 mapping.

4.3.5 S1

S1 is the main power switch for the Break-Out Board.

4.3.6 Reset

Pressing the Reset switch will cause a hardware reset on the CerfBoard SA1110. Note that this will not always reset the board: refer to the Intel Errata concerning Resets.

4.3.7 S3

DIP Switch S3 controls the GPIO buffer directions and output enables, as well as two fault indications to the SA-1110:

Switch Position	Function
S0	Not used
S1	Not used
S2	GPIO Port 2 Output Enable (closed or “1” is Disable)
S3	GPIO Port 2 Direction (closed or “1” is Output)
S4	GPIO Port 1 Output Enable (closed or “1” is Disable)
S5	GPIO Port 1 Direction (closed or “1” is Output)
S6	SA-1110 VDD Fault (closed or “1” indicates Fault is true)
S7	SA-1110 Batt Fault (closed or “1” indicates Fault is true)

Figure 42 - DIP Switch (S3) Settings

Note: When a 16-bit display is used, I/O-2 to I/O-9 are not available for GPIO use. Because the buffers are 8 bits wide, the remaining GPIOs must be used in output mode only. Thus S2 and S4 must be 1, or if they are open, S3 and S5 must be 1.

Shield

The shield is connected to the shields of all the Serial connectors, as well as the shields of the USB/Ethernet connectors on the CerfBoard SA1110.

Chapter 5 - Parts List

5.1 Cables

The **CerfBoard ODK** comes equipped with all of the cables required to connect to a host PC. The list of cables includes:

- The CerfBoard Serial Cable
- The Ethernet Patch Cable
- The Ethernet Crossover Cable

The rest of this section details the pinouts for the cables. The Ethernet Patch cable is commercially available; no pinout is provided.

5.1.1 CerfBoard Serial Cable

The CerfBoard serial cable uses three of the RS-232 standard signals–**RX**, **TX**, and **GND**. The two diagrams below show which of these pins are used. The image on the left of this diagram shows the connector that attaches to the serial header on the CerfBoard. Pin 1 on the CerfBoard is indicated by a "1" and a dot on the silkscreen.

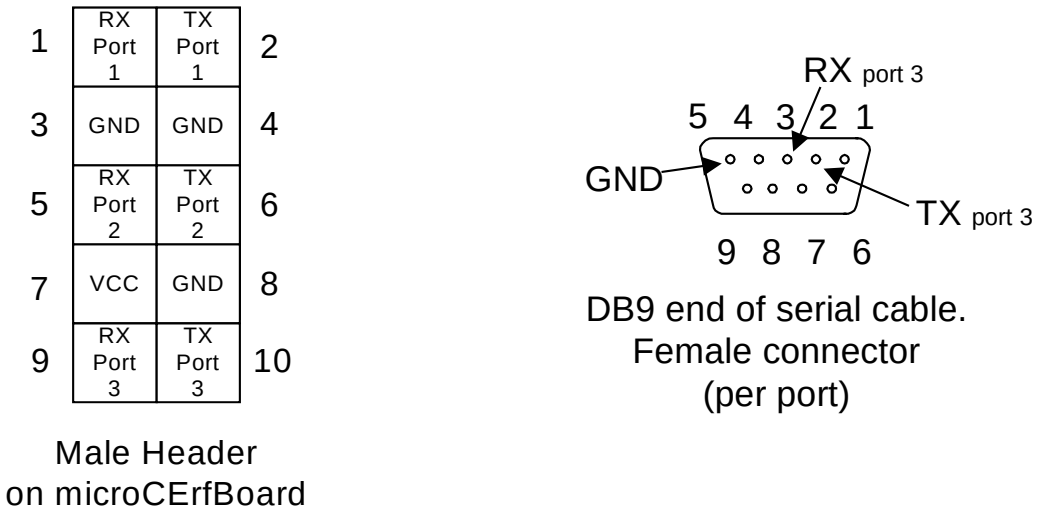

Figure 43 - CerfBoard Serial Cable Configuration

To connect the serial cable to the CerfBoard, locate pin 1 in the 2X5 female connector on the serial cable. Align the female connector with this pin to pin 1 of the corresponding male header on the CerfBoard.

5.1.2 Ethernet Crossover Cable

The Ethernet crossover cable is made from standard Category 5 UTP with 4 pairs. The pinout is as follows:

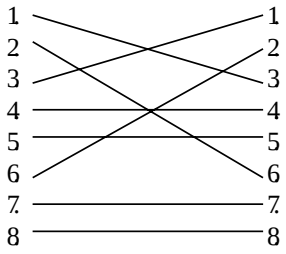

Figure 44 - Ethernet Crossover Cable

Note: It is also possible to use a commercial 2–pair crossover cable to connect the CerfBoard to a host PC.