CSE370: Introduction to Digital Design
Winter 1999

Homework Set 6

DUE: Feb 19, 1999, 12:30 pm

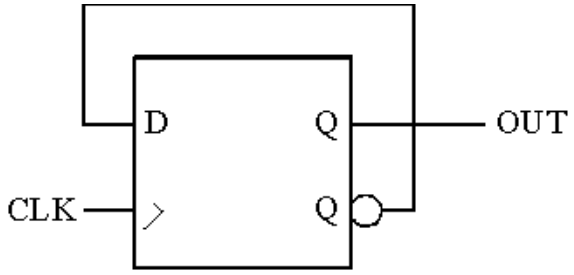
Please show *all* of your work. Solutions not involving DesignWorks do not have to be typeset, but may be if desired. In any case, your solutions must be legible.

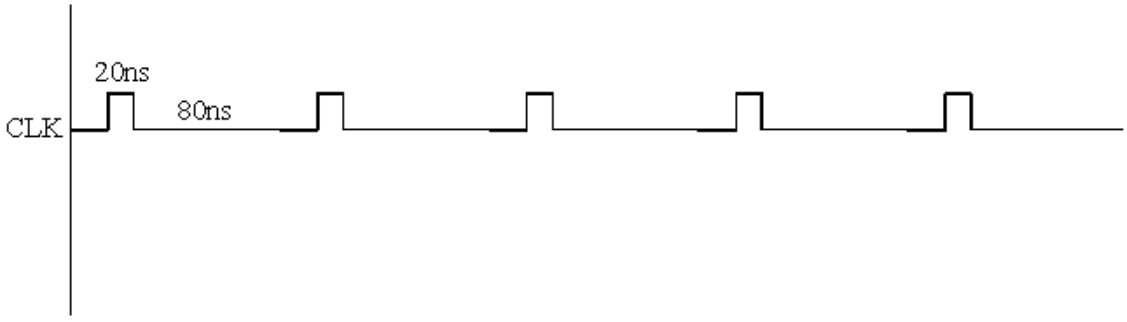
1) Katz problem 6.12 (a), (b), (c), and (d) [True/False questions about latches and flipiflops]. If your answer is FALSE, include a brief explanation of why.

2) Katz problem 6.11 (a), (b), and (c) [Timing diagram of D device].

3) Consider the following circuit and clock input as shown.
   a) Draw the timing diagram for OUT. Assume that OUT = 0 at time t = 0. Describe the function the circuit performs.

   b) In the waveform shown, the input clock is at a duty cycle of 20%. What would OUT's duty cycle be if the input clock's duty cycle were instead (a) 50% or (b) 80%?





4) Katz problem 6.22 [clocking issues].

5) You will now construct a fourth addition circuit to add to your growing library of adders developed for the homework assignments.
   a) Construct a 4-bit adder as a Verilog module in Designworks. Use the Verilog "+" operator to implement addition. Refer back to the tutorial on the web page to the section on how to get going with Verilog. Make sure that your module includes a carry-out. Turn in your Verilog source code
   b) Connect a keypad and probes to your adder block for testing. Verify that your adder works. Turn in printouts showing the following two tests:
      i) "1111" + "0001"
      ii) "1010" + "0101"