

Homework Set 5

DUE: Feb 12, 1999, 12:30 pm

Please show *all* of your work. Solutions not involving DesignWorks do not have to be typeset, but may be if desired. In any case, your solutions must be legible.

- 1) In problem 5 of homework set 3, you created a DesignWorks project for a binary full-adder. You drew the adder schematic, created a block symbol for the adder, verified that your adder functioned correctly, and cascaded four full adders to make the ripple-carry adder shown on pg. 249 of Katz. Now you will construct two additional adders for your library.
 - a) Construct a 4-bit carry-lookahead adder using pg. 255 of Katz as a reference. Use a reasonable level of modularization by creating your own sub-components as appropriate. For example, a flat schematic composed of a jumble of gates is probably not the most appropriate implementation just as a C program with only a main() routine and no functions would probably not be an optimal solution for most assignments in a software course. Turn in a DesignWorks schematics of your full-adder including the adder itself and the carry-lookahead logic. Verify that your adder operates correctly (you don't need to turn in schematics showing correct operation-- just verify that your circuit works right).
 - b) Construct an 8-bit carry-select adder. Use instances of your carry-lookahead adder from part a) in the implementation. Turn in a DesignWorks schematics. Verify that your adder operates correctly (you don't need to turn in schematics showing correct operation-- just verify that your circuit works right).
- 2) Katz exercise 5.16. Recall that "bit-slice" in this context just means that you have two single bit inputs and one single bit output. The idea is that if you were subsequently asked to make a 4 bit ALU, you could take your solution for one "bit-slice" and simply group 4 of them together. Your circuit should have 6 inputs (S0, S1, S2, A, B, Cin) and 2 outputs (Out and Cout), but clearly not all 6 I/O lines will be used by some of the operations. Turn in DesignWorks schematics of your circuit. As in problem 1) you should take whatever steps you feel are necessary to verify that your ALU operates correctly but you don't need to turn in schematics showing correct operation.
- 3) Fill in the output waveforms Q and Q' for the following circuit given the inputs A and B. Assume that each tick mark on the waveform graph represents 4 NAND-gate delays. In a concise paragraph, compare and contrast the behavior of this circuit with the cross-coupled NOR gates shown on pgs. 286-287 of the text.

