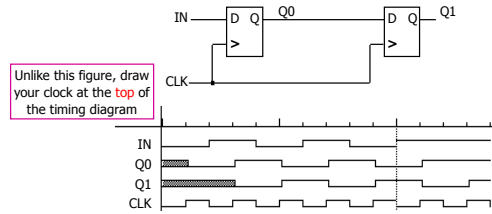


Overview

- ◆ Last lecture
 - Review of D latches and flip-flops
 - T flip-flops and SR latches
 - State diagrams
 - Asynchronous inputs
- ◆ Today
 - Cascading flip-flops
 - Clock skew
 - Registers

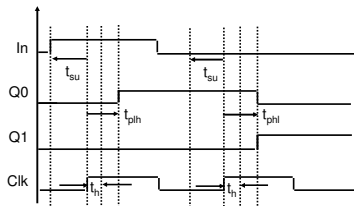
Cascading flip-flops

- ◆ Example: Shift registers
 - First FF acquires IN at rising clock edge
 - Second FF acquires Q0 at rising clock edge



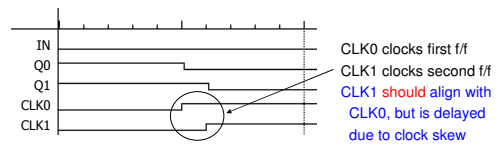
Cascading flip-flops (con't)

- ◆ Flip-flop propagation delays exceed hold times
 - Second stage latches its input before input changes



Clock skew

- ◆ Goal: Clock all flip-flops at the same time
 - Difficult to achieve in high-speed systems
 - Clock delays (wire, buffers) are comparable to logic delays
 - Problem is called **clock skew**

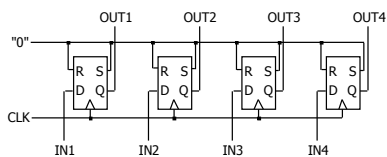


Original state: IN = 0, Q0 = 1, Q1 = 1
 Next state: Q0 = 0, Q1 = 0 (should be Q1 = 1)

Registers

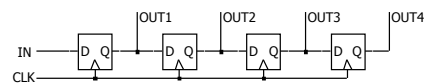
- ◆ Collection of flip-flops with common control
 - Store related values (e.g. a binary word)
 - Share clock, reset, and set lines
 - Examples
 - Storage registers, shift registers, counters

Example:
A 4-bit
storage
register



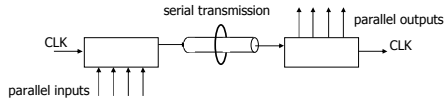
Shift registers

- ◆ Hold successively sampled input values
 - Delays values in time
 - Example: 4-bit shift register
 - Stores 4 input values in sequence

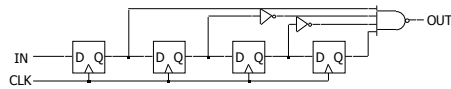


Shift-register applications

- ◆ Parallel-to-serial conversion for signal transmission



- ◆ Pattern recognition (circuit recognizes 1001)

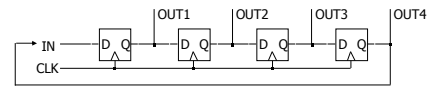


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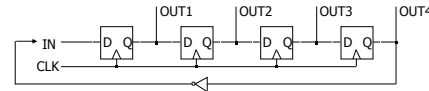
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Counters

- ◆ Ring counter: Sequence is 1000, 0100, 0010, 0001
 - Assuming one of these patterns is the starting state



- ◆ Johnson counter: Sequence is 1000, 1100, 1110, 1111, 0111, 0011, 0001, 0000

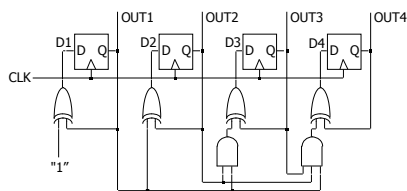


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Class example: A binary counter

- ◆ Has logic between flip-flops
 - Draw a timing diagram



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Summary: Sequential-logic building blocks

- ◆ Know latches and flip-flops
 - R-S latch
 - D latch and D flip-flop
 - Master/slave flip-flops
 - T flip-flop
- ◆ Know clocks, timing, timing diagrams
 - Flip-flop timing and delay specifications
 - Clock skew
- ◆ Understand asynchronous inputs
 - Metastability and how to avoid it
- ◆ Know basic registers
 - Storage registers, shift registers, counters

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