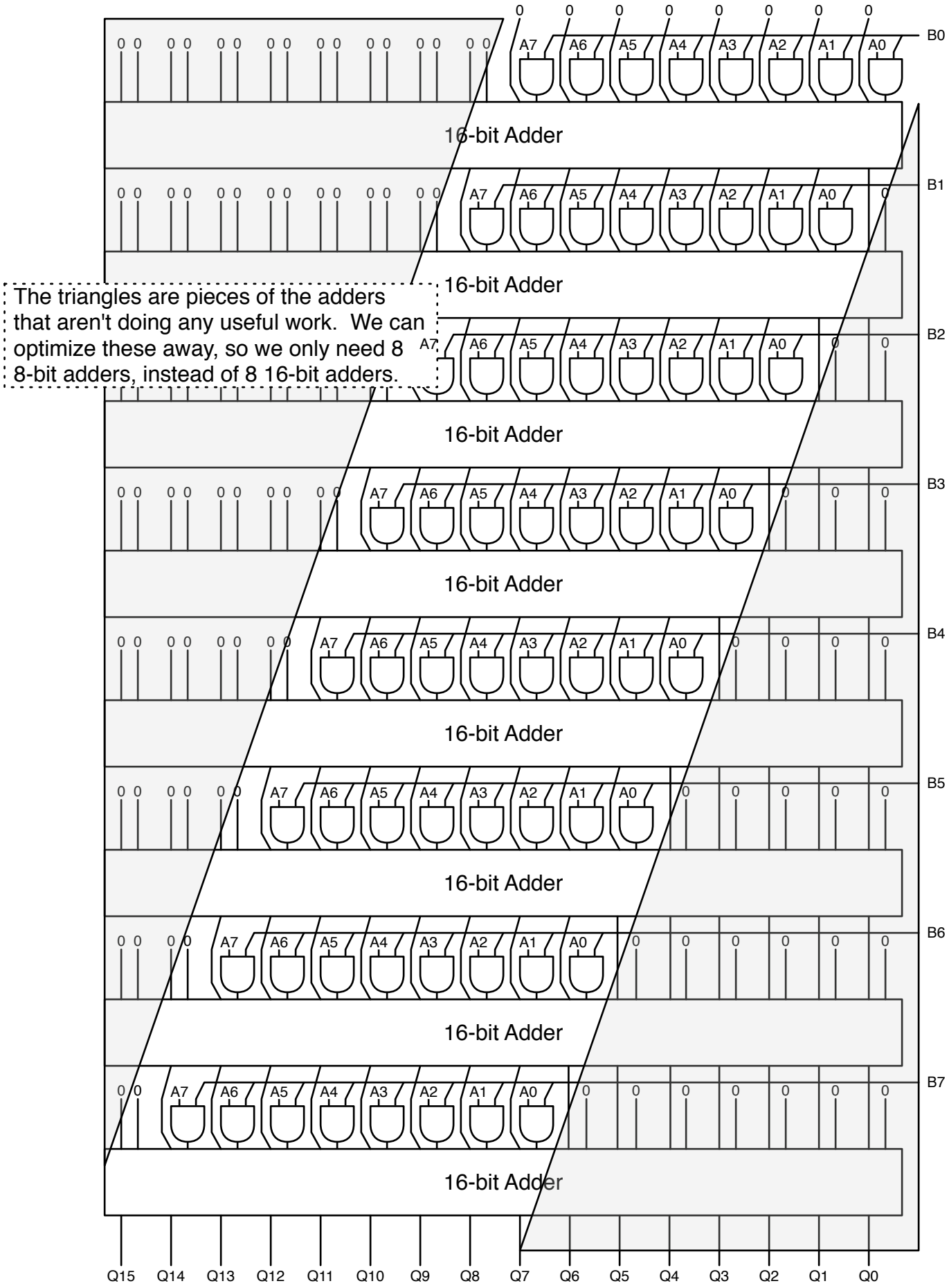
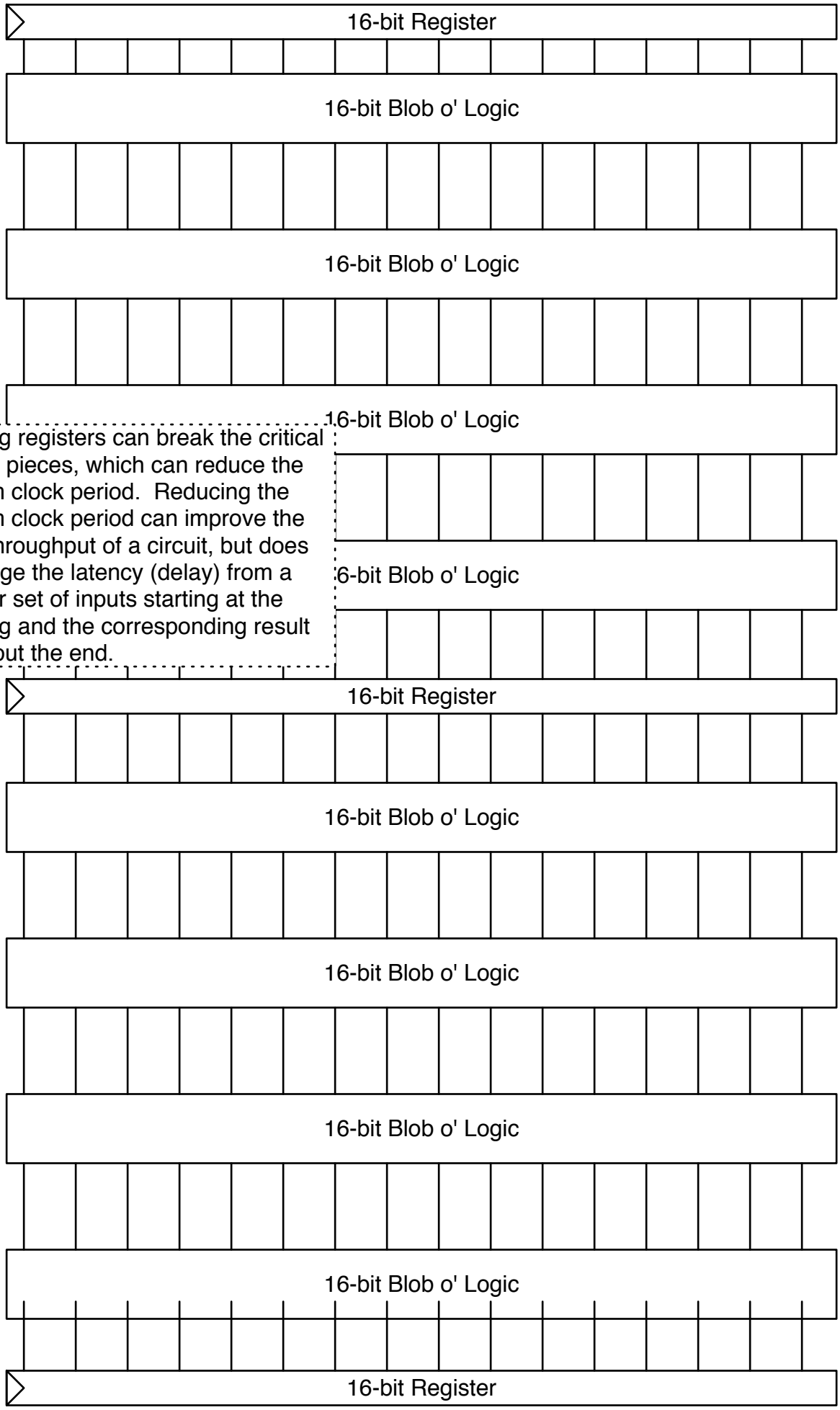
Combinational "shift and add" multiplier



Pipelining



Pipelining registers can break the critical path into pieces, which can reduce the minimum clock period. Reducing the minimum clock period can improve the overall throughput of a circuit, but does not change the latency (delay) from a particular set of inputs starting at the beginning and the corresponding result coming out the end.

The Wallace Tree