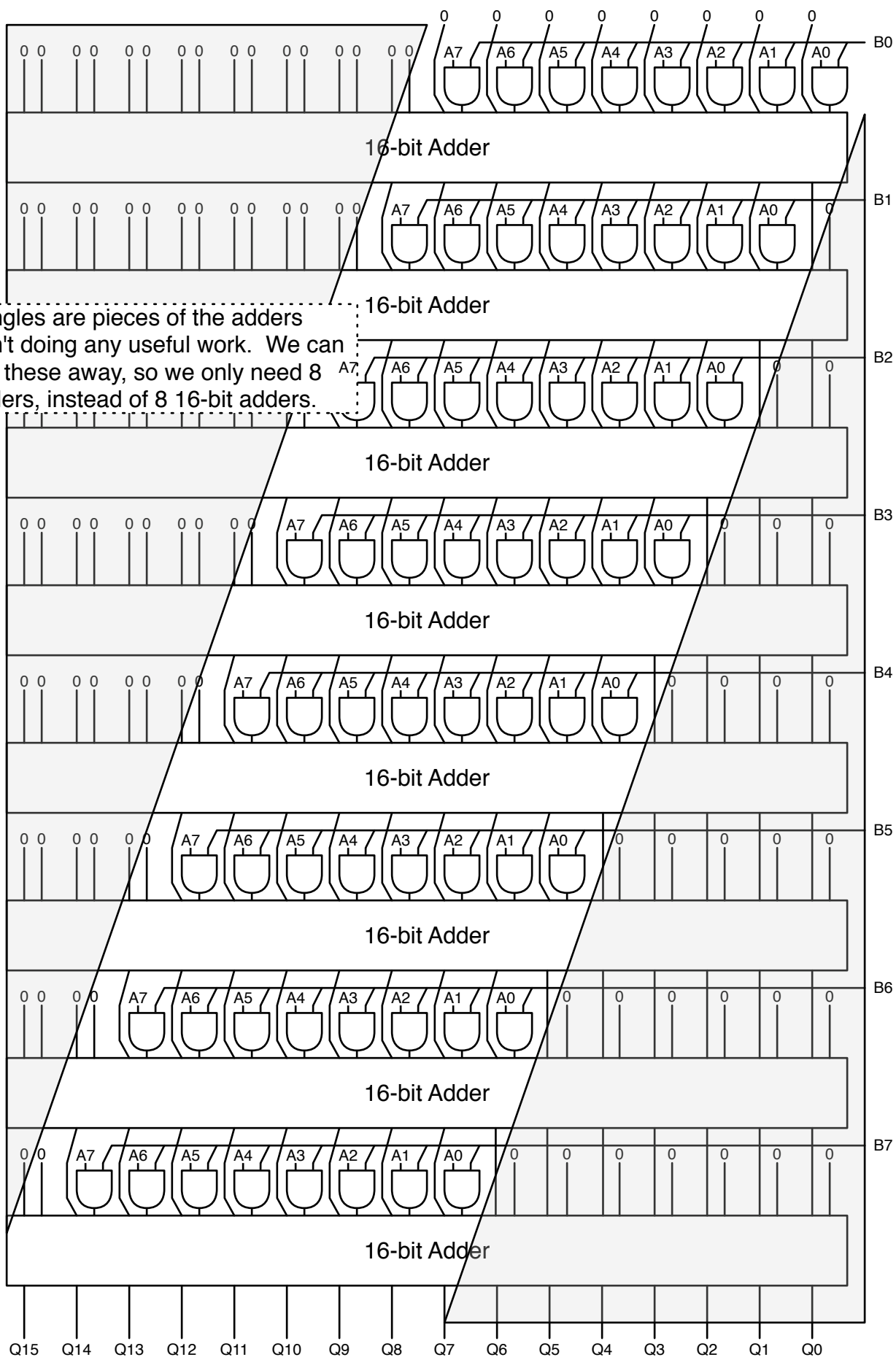
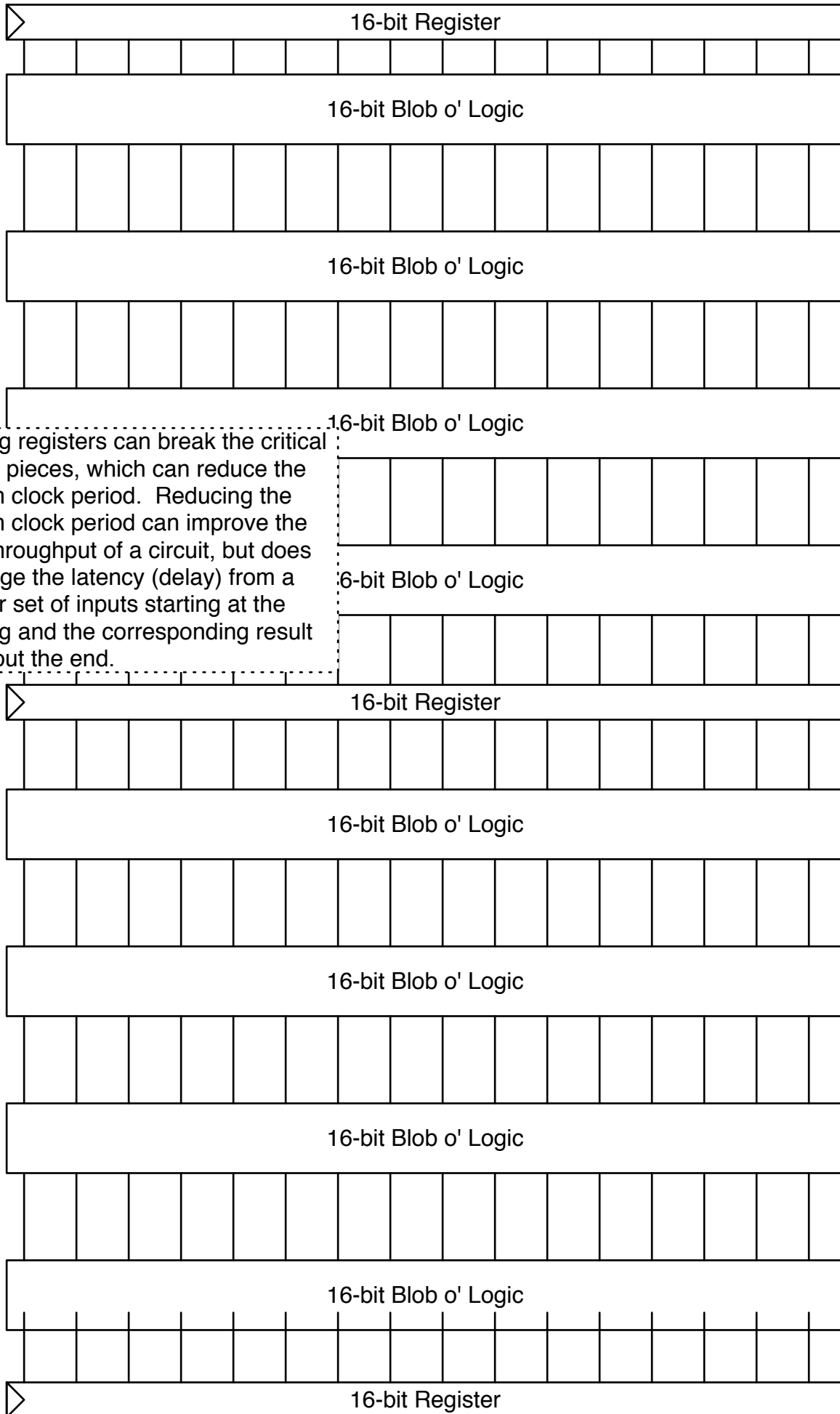


Combinational "shift and add" multiplier

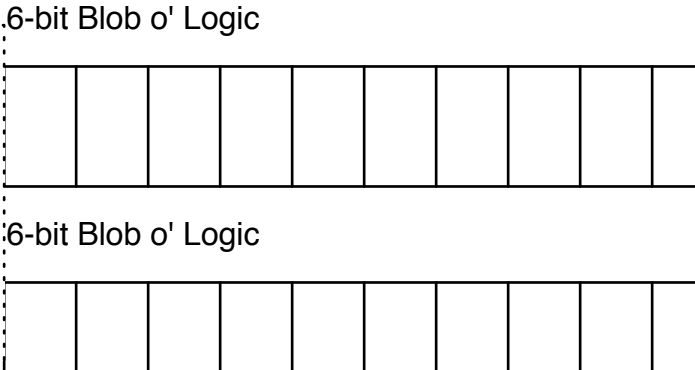


The triangles are pieces of the adders that aren't doing any useful work. We can optimize these away, so we only need 8 8-bit adders, instead of 8 16-bit adders.

Pipelining



Pipelining registers can break the critical path into pieces, which can reduce the minimum clock period. Reducing the minimum clock period can improve the overall throughput of a circuit, but does not change the latency (delay) from a particular set of inputs starting at the beginning and the corresponding result coming out the end.



The Wallace Tree

