# Lecture 12: Time and Glitches

CSE 370, Autumn 2007
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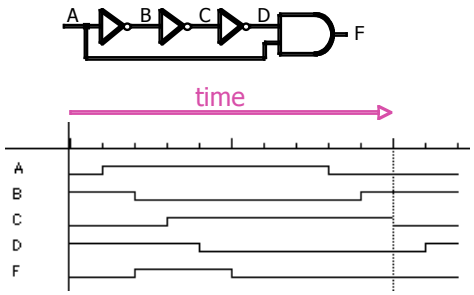
## Where We Are

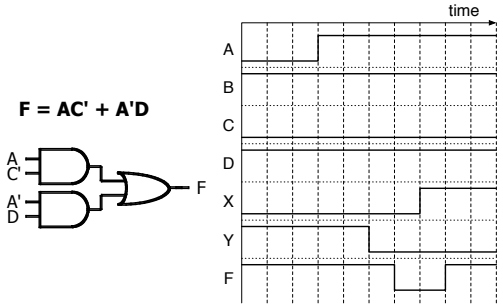
- Last lecture: Multi-Level Logic
- This lecture: Circuit Delay and Timing
- Next lecture: Adders, Comparators, ALUs
- Exam 1 on Wednesday
- Homework 4 in progress
- Lab 4 this week



## Sometimes Time Matters

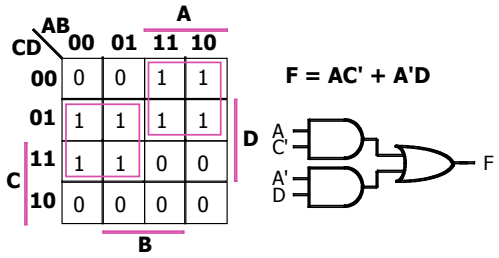


# Glitches and Hazards



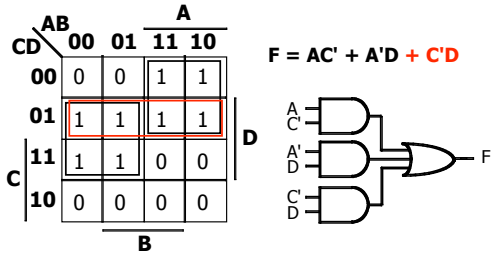



# Where Glitches Come From

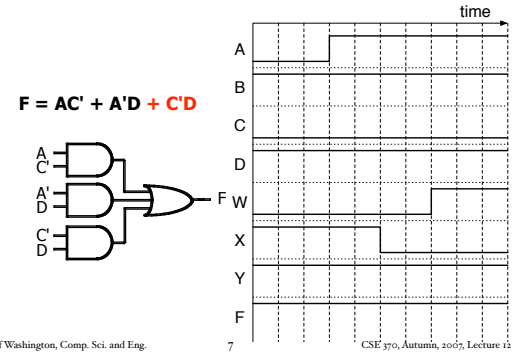





# Avoiding Glitches in 2-Level Circuits



## Additional Gate Prevents Glitches



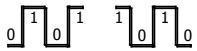



## Terminology of Hazards

- Static 1-Hazard

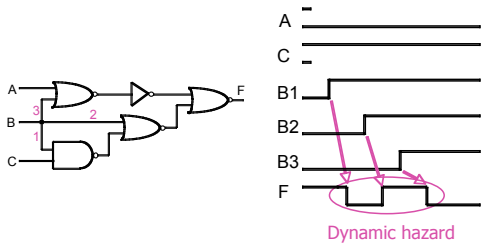

- Static 0-Hazard


- Dynamic Hazards






## A Dynamic Hazard



## Avoiding Dynamic Hazards

- Very hard
- Automated tools can help
- In practice, use 2-level circuits if you must avoid hazards at all costs



## Now You Try

- F(A,B,C,D) = ¬AB + A¬CD + ¬BCD
- Draw waves that illustrate one input pattern/ transition that can cause a glitch, and identify which gates would have to be slow or fast
- Change the circuit to make it hazard-free and draw the resulting circuit



## Thank You for Your Attention

- Read lab 4
- Study for the exam
- Continue working on homework 4
- Continue reading the book