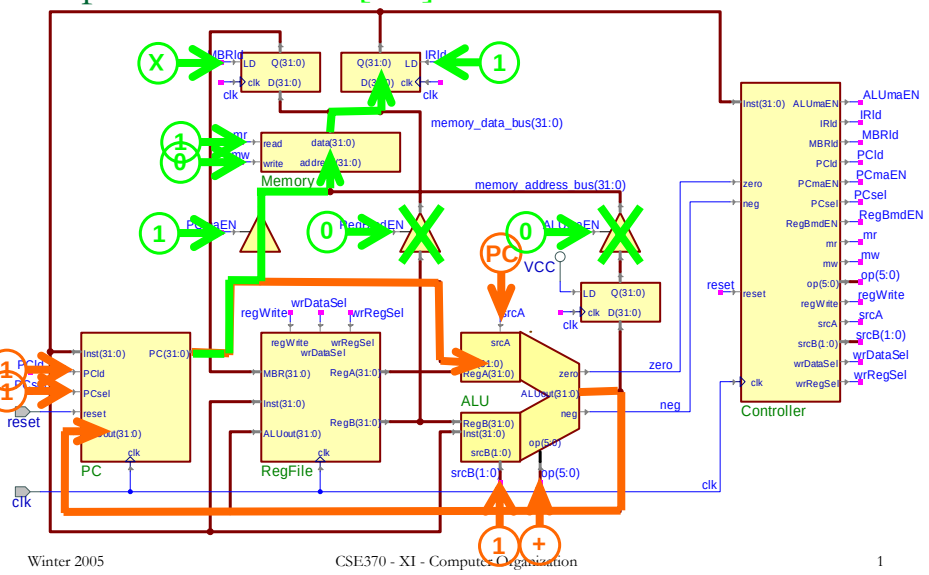
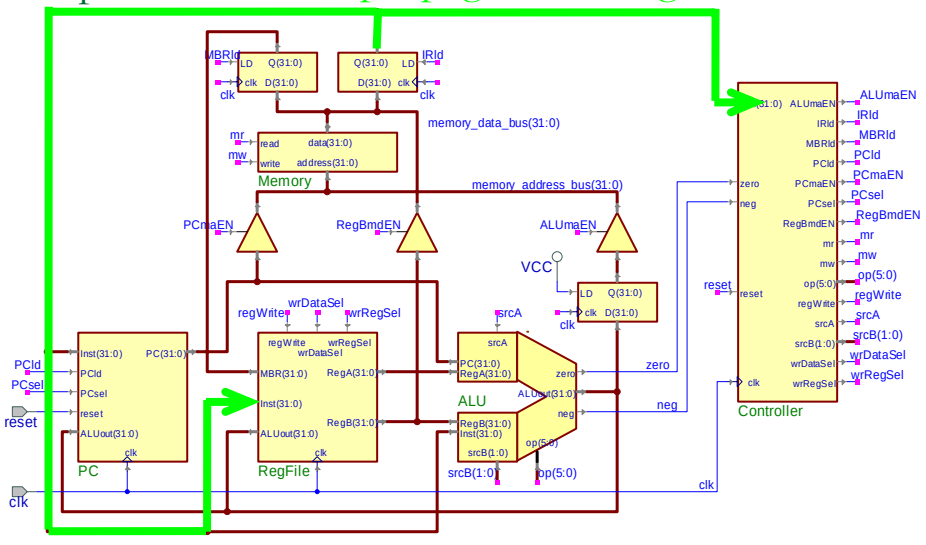
Tracing an instruction's execution (LW)

Step 1: IR ← mem[PC]; PC ← PC + 1;



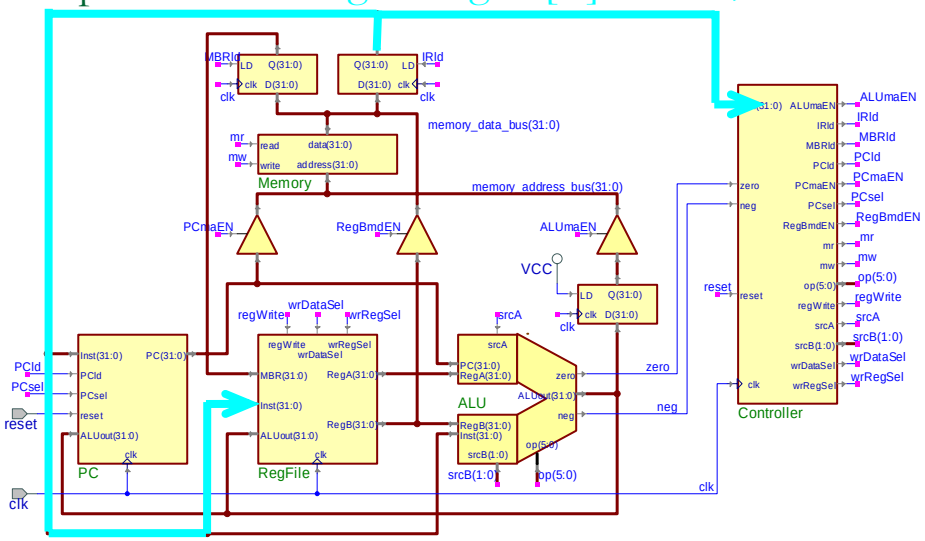
Tracing an instruction's execution (LW cont'd)

Step 2: Instruction propagates through controller



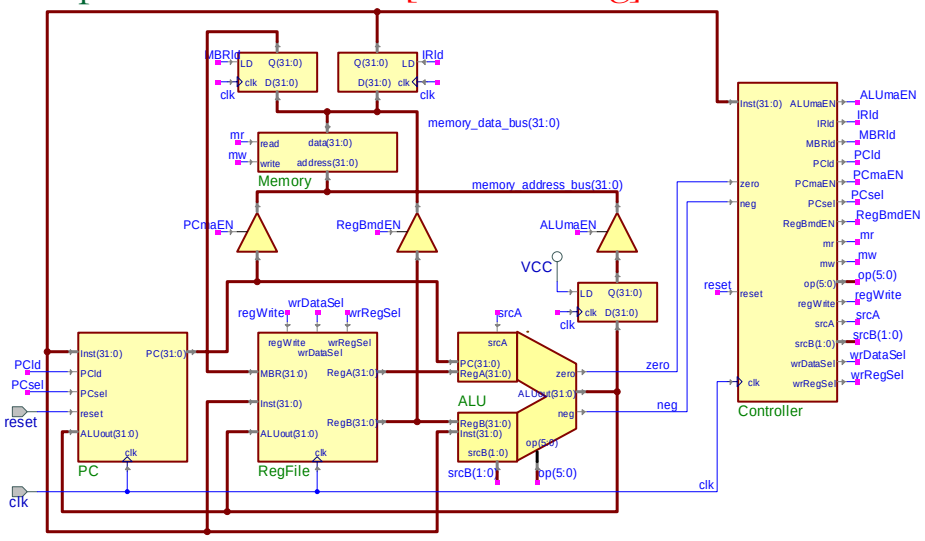
Tracing an instruction's execution (LW cont'd)

Step 3: ALUoutReg ← regfile[rs]+offset;



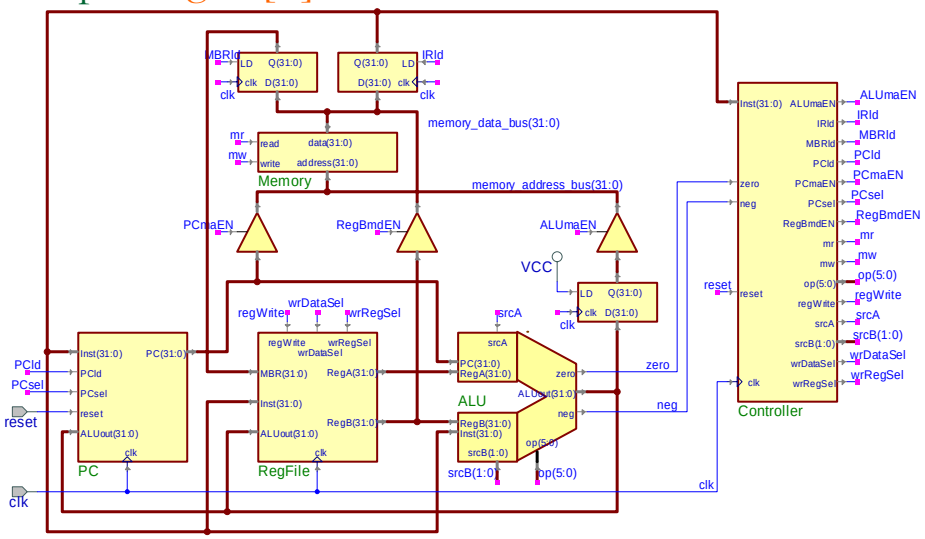
Tracing an instruction's execution (LW cont'd)

Step 4: MBR ← mem[ALUoutReg];



Tracing an instruction's execution (LW cont'd)

Step 5: regfile[rt] ← MBR;



Controller signals for all cycles (LW cont'd)

Control signals for:	Fetch	Decode	LW1	LW2	LW3
PCmaEN =	1	0			
ALUmaEN =	0	0			
RegBmdEN =	0	0			
mr =	1	X			
mw =	0	0			
IRld =	1	0			
MBRld =	X	X			
srcA =	"PC"	X			
srcB =	"1"	X			
op =	"+"	X			
regWrite =	0	0			
wrDataSel =	X	X			
wrRegSel =	X	X			
PCld =	1	0			
PCsel =	1	X			