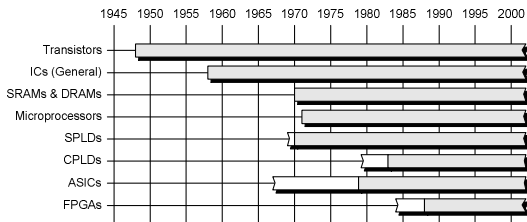
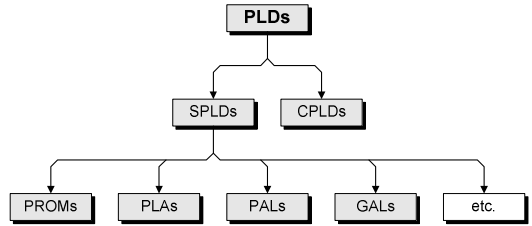


Evolution of FPGA Hardware

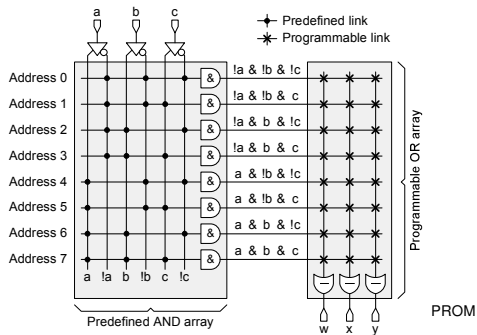


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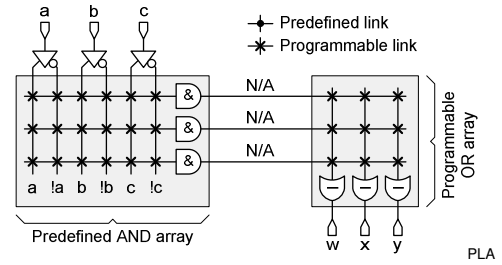
PLDs



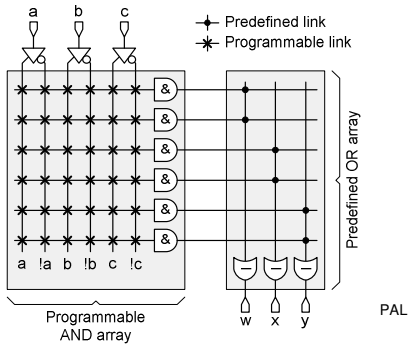
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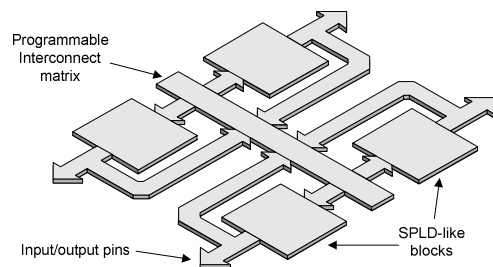


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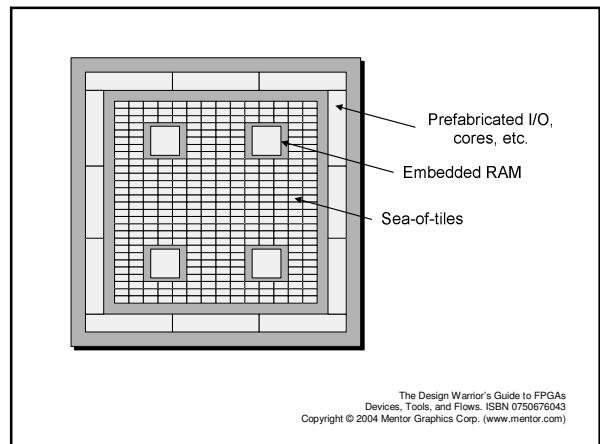
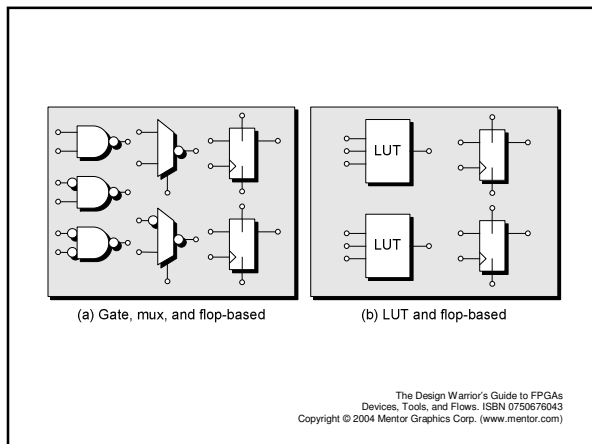
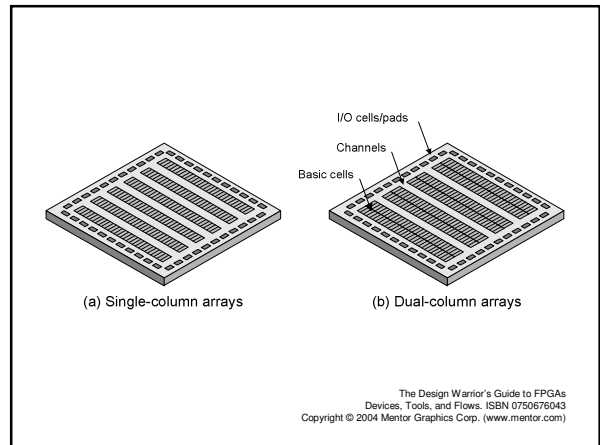
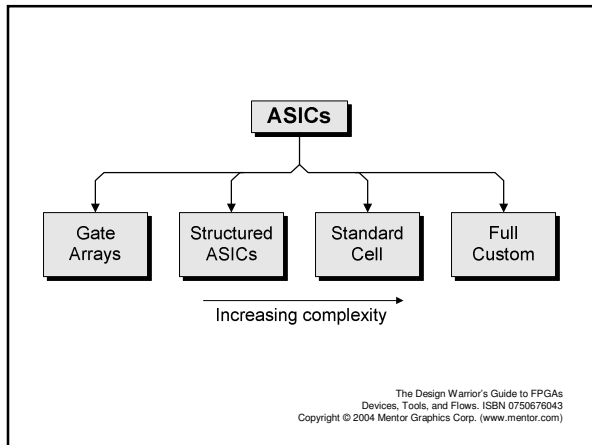
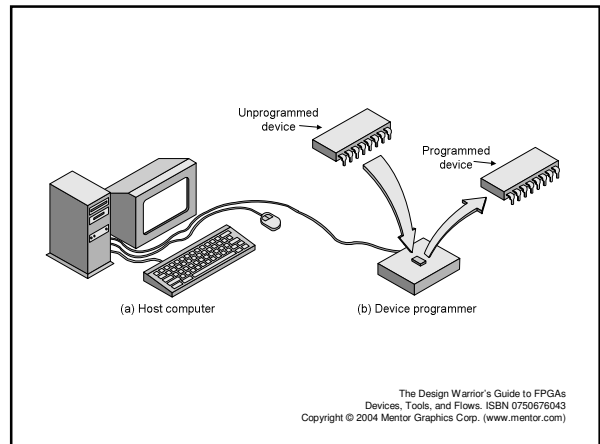
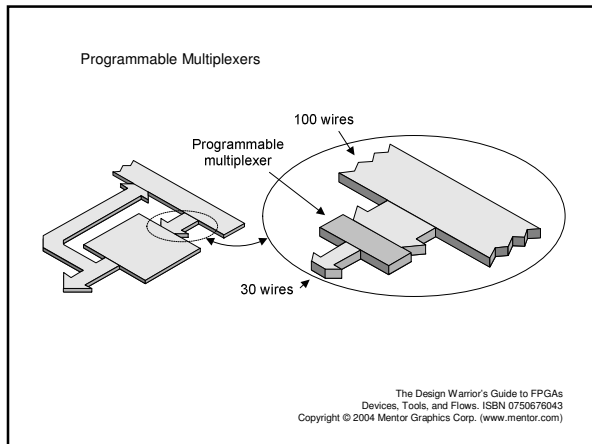


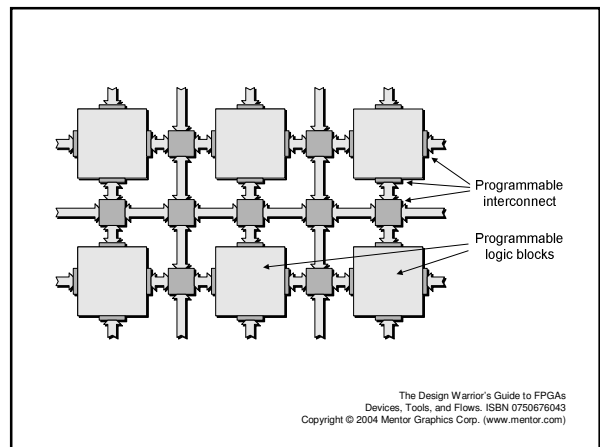
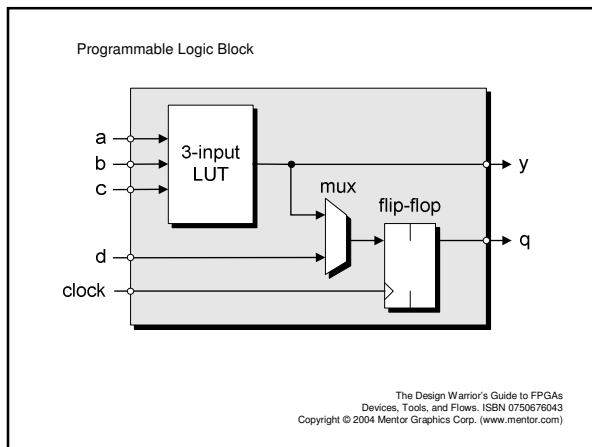
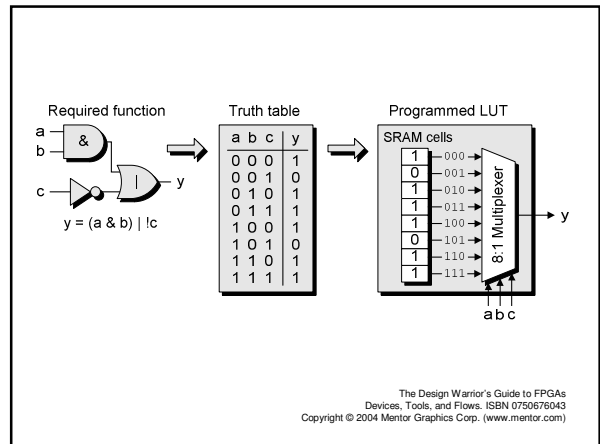
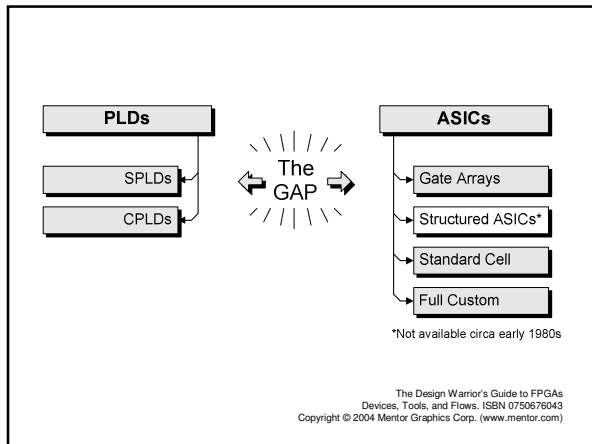
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Generic PLD Structure



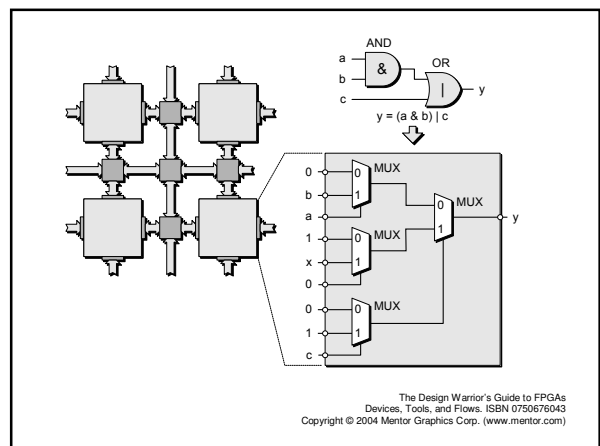
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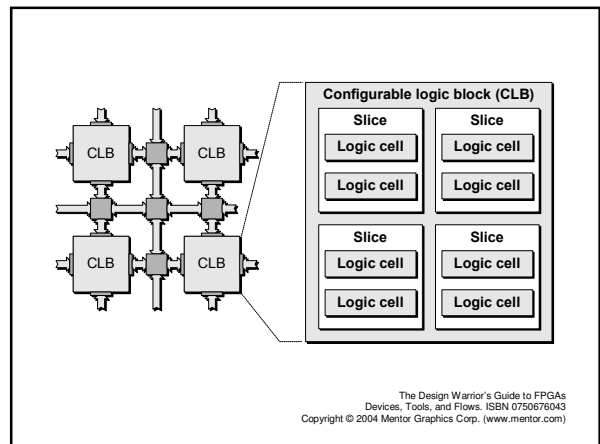
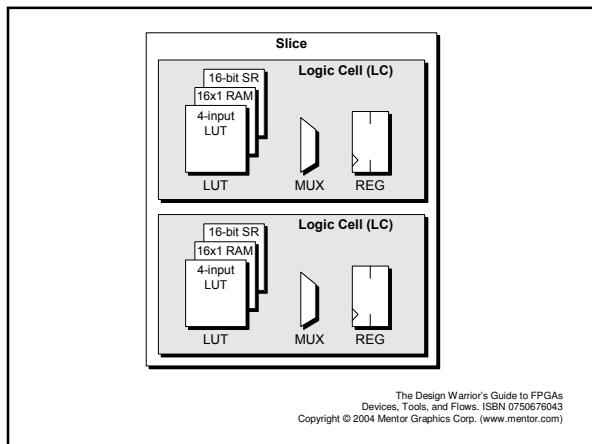
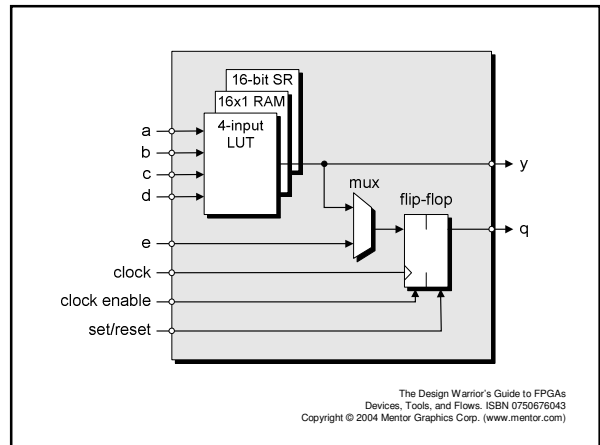
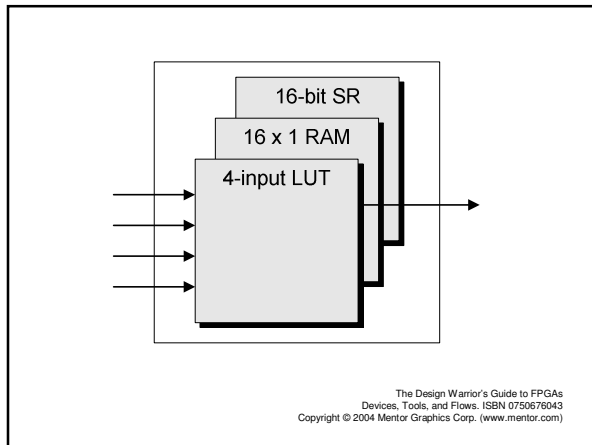
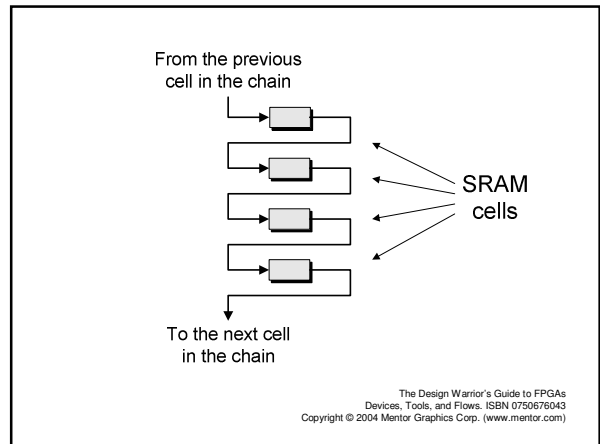
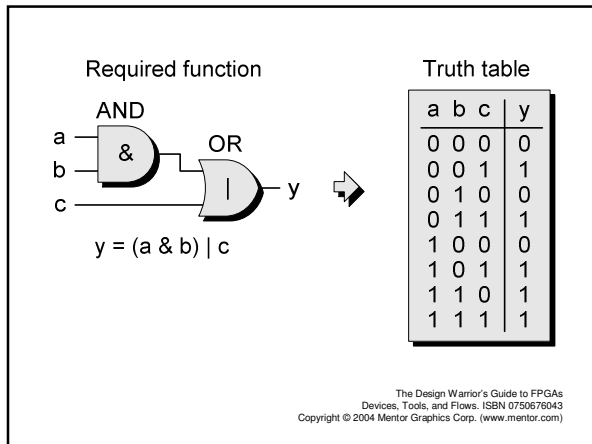


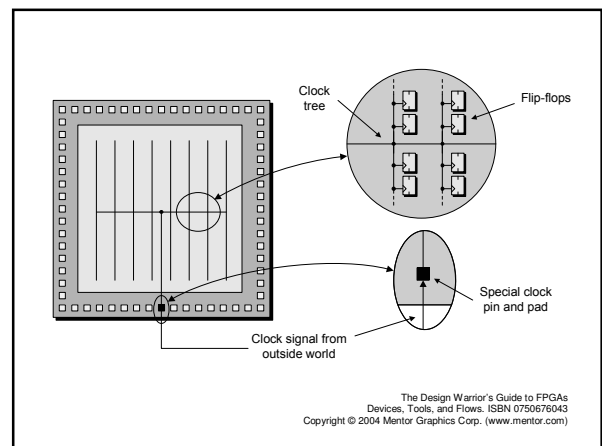
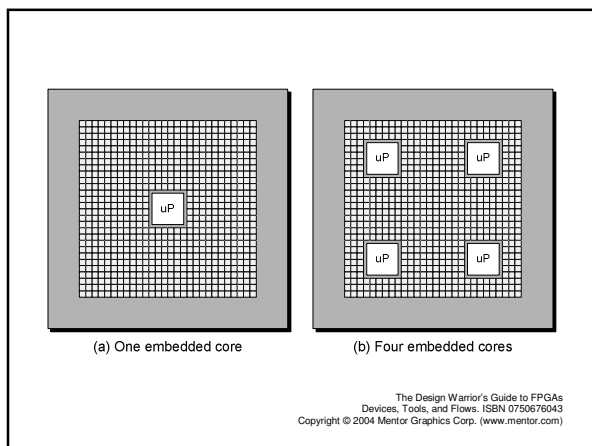
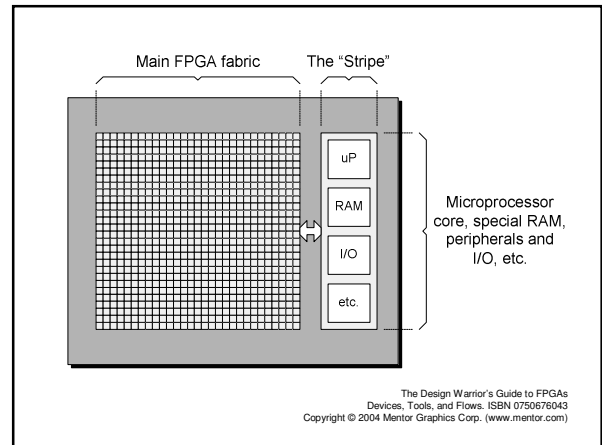
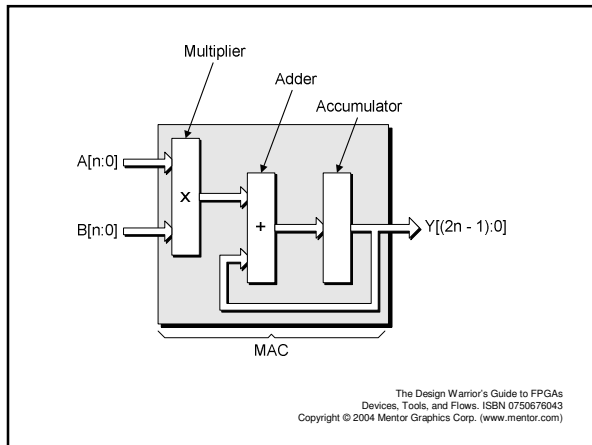
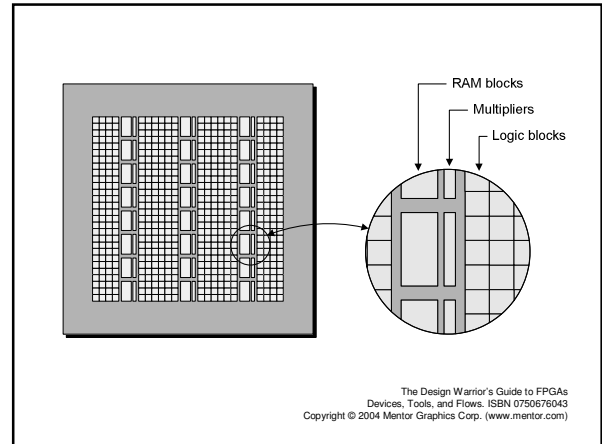
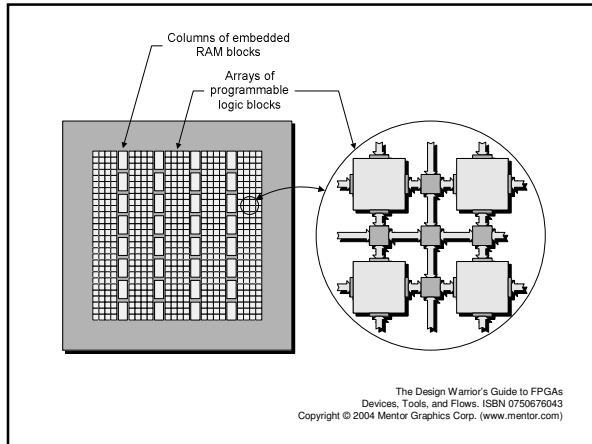


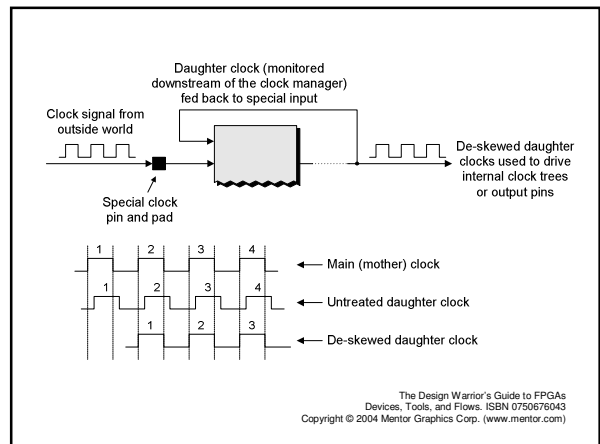
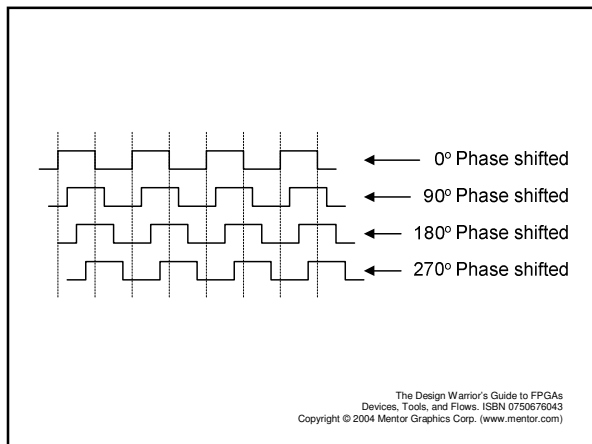
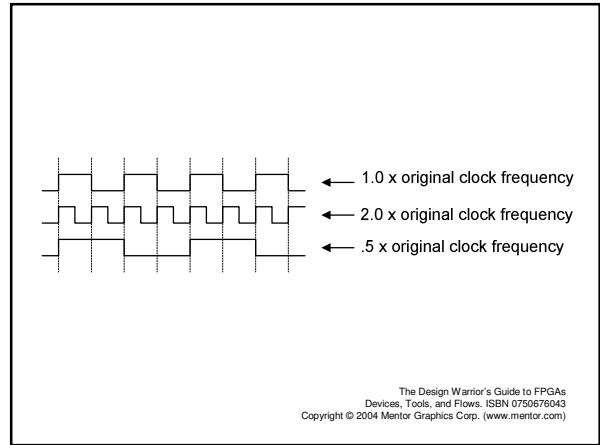
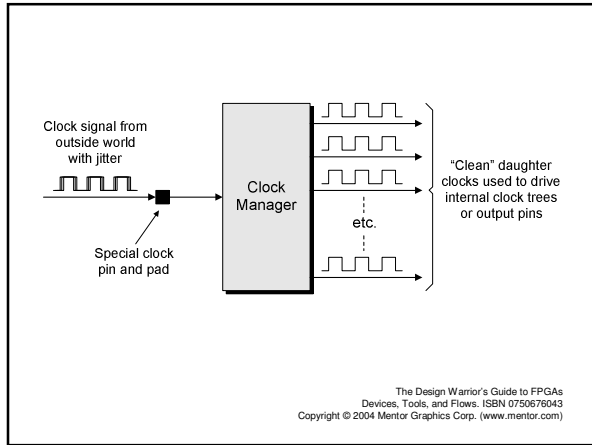
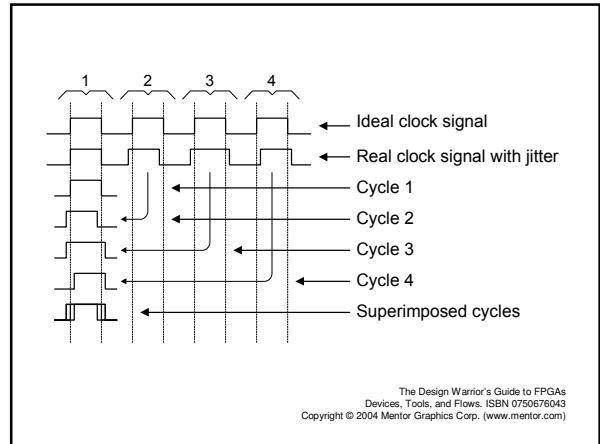
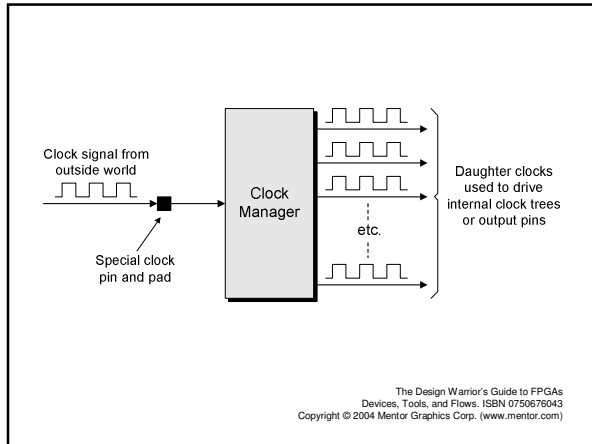
Feature	SRAM	Antifuse	EEPROM / FLASH
Technology node	State-of-the-art	One or more generations behind	One or more generations behind
Reprogrammable	Yes (in system)	No	Yes (in-system or offline)
Reprogramming speed (inc. erasing)	Fast	---	3x slower than SRAM
Volatile (must be programmed on power-up)	Yes	No	No (but can be if required)
Requires external configuration file	Yes	No	No
Good for prototyping	Yes (very good)	No	Yes (reasonable)
Instant-on	No	Yes	Yes
IP Security	Acceptable (especially when using bitstream encryption)	Very Good	Very Good
Size of configuration cell	Large (six transistors)	Very small	Medium-small (two transistors)
Power consumption	Medium	Low	Medium
Rad Hard	No	Yes	Not really

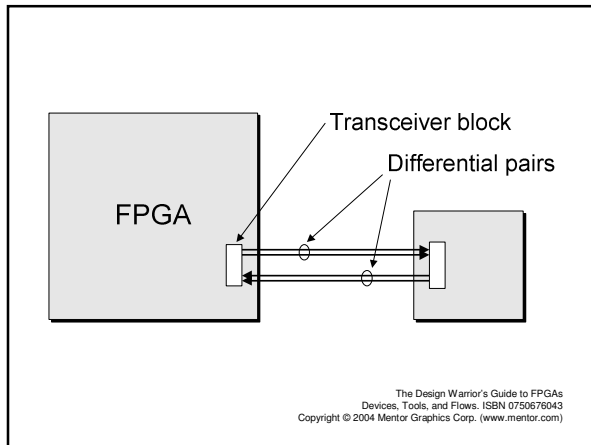
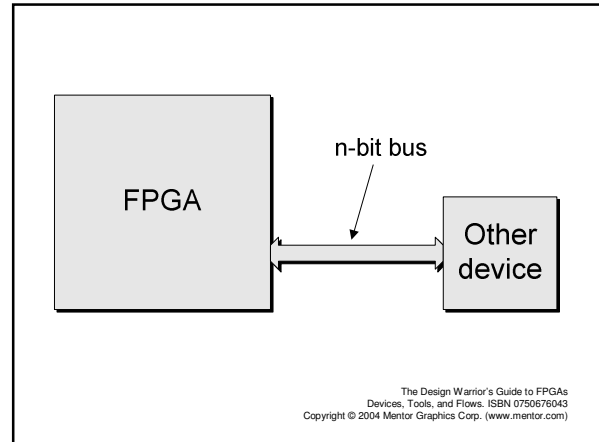
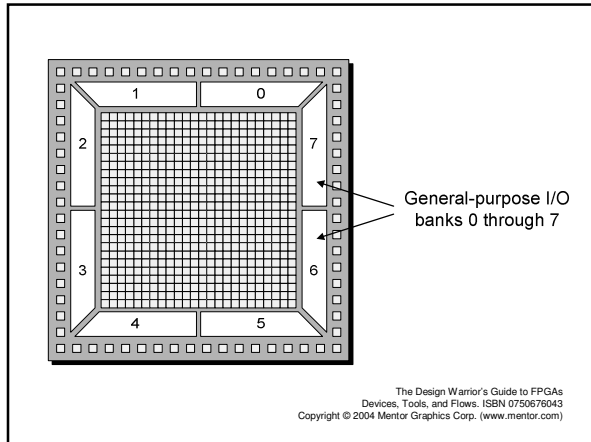
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- ## Computer-aided Design
- Can't design FPGAs by hand
 - way too much logic to manage, hard to make changes
 - Hardware description languages
 - specify functionality of logic at a high level
 - Validation - high-level simulation to catch specification errors
 - verify pin-outs and connections to other system components
 - low-level to verify mapping and check performance
 - Logic synthesis
 - process of compiling HDL program into logic gates and flip-flops
 - Technology mapping
 - map the logic onto elements available in the implementation technology (LUTs for Xilinx FPGAs)
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- ## Applications of FPGAs
- Implementation of random logic
 - easier changes at system-level (one device is modified)
 - can eliminate need for full-custom chips
 - Prototyping
 - ensemble of gate arrays used to emulate a circuit to be manufactured
 - get more/better/faster debugging done than possible with simulation
 - Reconfigurable hardware
 - one hardware block used to implement more than one function
 - functions must be mutually-exclusive in time
 - can greatly reduce cost while enhancing flexibility
 - RAM-based only option
 - Special-purpose computation engines
 - hardware dedicated to solving one problem (or class of problems)
 - accelerators attached to general-purpose computers
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