

Name: _____

CS370: Introduction to Digital Design

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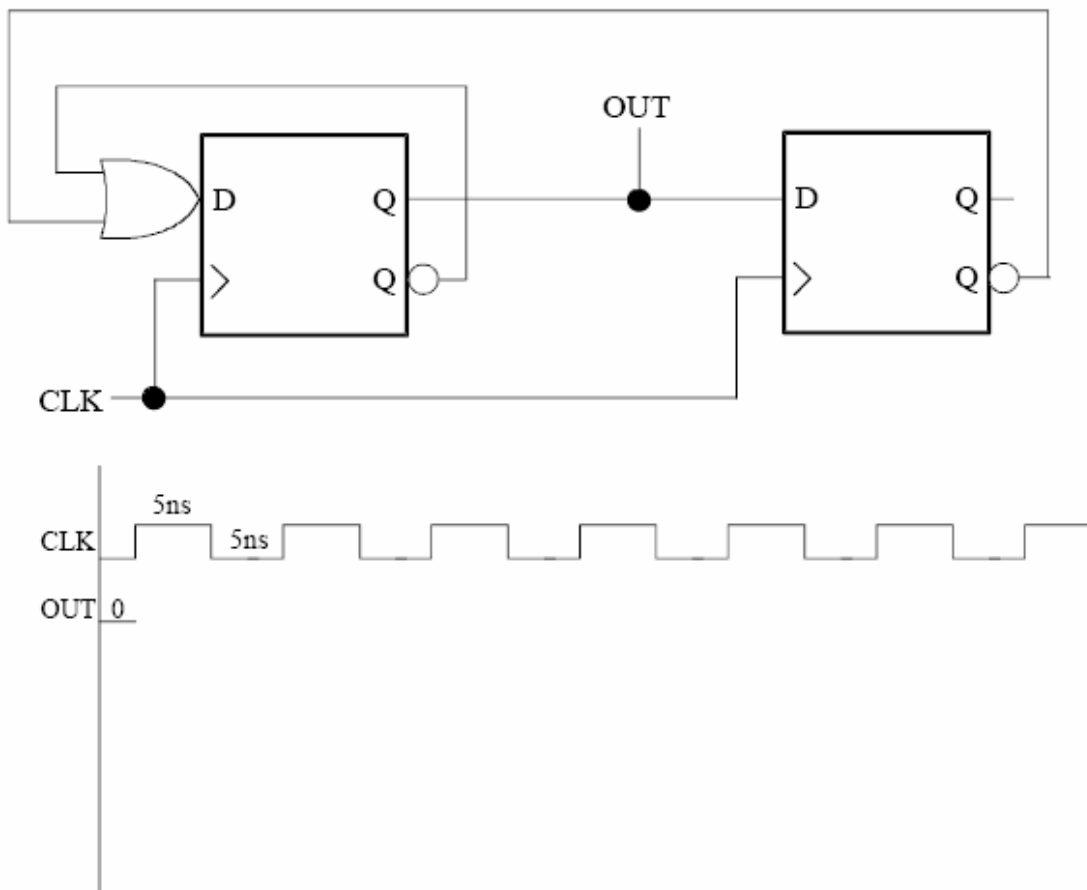
Quiz #3 -- Take home version

November 10, 2004

Quiz Policy:

No collaboration. Your solutions are due in class Friday, Nov. 12. Please write your answers on this sheet (front and back).

1. You are given the following circuit



(a) (8 pts) Assuming a clock input as shown, and that $OUT = (\text{logic } 0)$ at time $t = 0\text{ns}$, draw a timing diagram. Label and draw OUT 's timing, and also show the timing for any internal nodes that you use to derive OUT .

(b) (4 pts) What is OUT 's duty cycle? _____

- (c) (4 pts) The clock frequency is 100MHz. Indicate by checking either (y) or (n) whether flip-flops with the following propagation delays, setup times, and hold times will work satisfactorily in this circuit. Assume that the OR gate has zero propagation delay.

(y) (n)	Propagation delay	Setup time	Hold time
() ()	10ns	10ns	10ns
() ()	5ns	5ns	5ns
() ()	6ns	2ns	6ns
() ()	6ns	6ns	2ns

2. Identify the following statements as being either true or false. Each question is worth 2 pts.

- () T/F? Applying $S=0$ and $R=0$ to an S-R latch is an invalid input, because the output can enter a race condition.
- () T/F? A flip-flop's propagation delay, from a change in the clock edge to a change in the output, typically is shorter than the flip-flop's hold time, so you can construct shift registers from cascaded flip-flops.
- () T/F? Assuming zero setup and hold times, clocked latches and flip-flops produce the same outputs as long as the inputs do not change while the clock is asserted high.

3. Given the verilog snippets below, answer the questions:

reg B, C, D;

```
always @(posedge clk)
begin
  B = A;
  C = B;
  D = C;
end
```

- a) (2 points) after executing, D=original value of _____. b) (2 points) is this **blocking** or **non-blocking**?

reg B, C, D;

```
always @(posedge clk)
begin
  B <= A;
  C <= B;
  D <= C;
end
```

- c) (2 points) after executing, D=original value of _____. d) (2 points) is this **blocking** or **non-blocking**?