Practice problems

CSE 370 Quiz section
01/27/2000

Warm up

Fast K-Maps. Emphasis on FAST!

CD \ AB	00	01	11	10
00	0	0	1	1
01	0	1	1	X
11	X	0	0	0
10	X	0	1	1

CD \ AB	00	01	11	10
00	1	X	1	X
01	0	X	0	X
11	1	1	1	0
10	0	1	0	1

CD \ AB	00	01	11	10
00	1	0	1	0
01	0	1	0	1
11	1	0	1	0
10	0	1	0	1

CD \ AB	00	01	11	10
00	1	0	0	0
01	1	0	X	1
11	X	1	1	0
10	0	0	0	0

Problem 1

You just bought a new 64-bit state of the art computer from GoatWay: dual Zentium VII 2 GHZ, 40 Gigs of HD, etc. Unfortunately, the people at GoatWay are silly, and they gave you only 16 Megs of RAM! Going through some of your old stuff, you find hidden in your cupboard 4 old pieces of RAM. Each piece of RAM is byte addressable and has 22 address wires.

a) How much RAM is there in one of these chips of RAM?
b) How many address wires are required to access your 16 Megs of RAM on your new computer?
c) You really want to install those old RAM chips in your new computer. Design the hardware needed to do this (hint: use multiplexors)

Problem 2

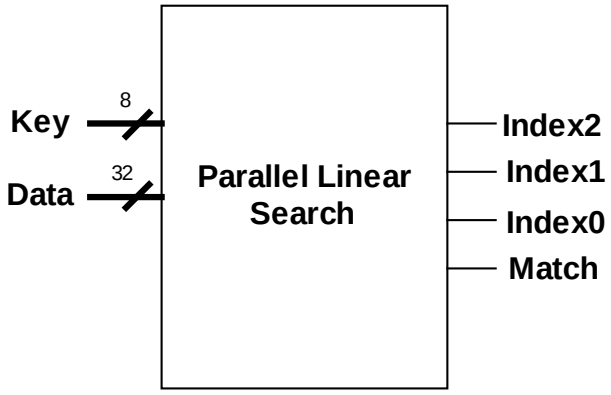
MMX is an instruction set that the Intel Pentium chips support. MMX provides instructions that work on data in parallel. For example, if I give the Pentium chip 8 pairs of integers, the chip can add these pairs in parallel, giving me 8 results.

Your new startup company has done a lot of research on programming styles, reaching the conclusion that ALL programmers out there are REALLY lazy, and because of that they often use linear search to find things in an array (instead of using more sophisticated data structures such as hash tables).

So, in order to make linear search a lot faster, you've decided that the new processor you will manufacture, the Pherced, will have a parallel linear search instruction (and this will be *far* better than MMX). The instruction will take one 8-bit key, and a 32 bit number, which represents an array of 4 8-bit integers. The instruction searches in parallel for the given key in the array, and if a match is found, it returns the index of the match in the array.

Design the following block, which will be used in your new processor to implement the parallel linear search instruction.

Notes on input/output behavior: Key and Data are obvious. On the output, Match should be 1 if there is a match, 0 otherwise. If Match is 1, Index[2..1] should contain the index into data where the key was found (000 means index was found at Data[0..7])



Problem 3

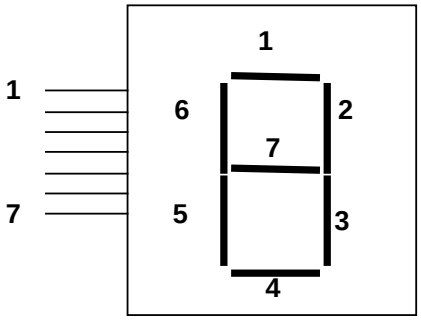
The very well known Snorkel function is defined as follows:

Snorkel(A, B, C, D) = A'BCD + ABC'D + AC

a) Implement the Snorkel function using a 16:1 Multiplexor.
b) Implement your 16:1 Multiplexor using gates (Hint: divide and conquer)
c) Design a circuit for the Snorkel function using a minimum number of gates.
d) Compare the number of gates used in your design from part a and b with the one from part c. Also compare the propagation delay of your two designs, assuming all gates have the same propagation delay T_p. Which one is better?

Problem 4

You have to design the graphical display for an elevator. The elevator control system, already designed by Microsoft (which has now gone into the hardware market) will give you a 4-bit number which will represent the state that the elevator is in. You have to use a 7-segment display, as shown below, to display information about the elevator. The seven-segment display has 7 inputs, one for each segment. When a given input is 1, the associated segment is turned on, when it's 0, the associated segment is turned off.



The states that the elevator can be in are sequentially numbered from 0 up to 10, and are: Up, Down, Burning (in case the users haven't noticed that the elevator is burning…), 0 (floor 0…), 1 (1st floor), 2, 3, 4, 5, 6, 7.

Design a block that will use the 4 bit state given by the elevator controller to generate the inputs to the seven segment display (Represent Up as 'U', Down as 'd', Burning as 'b', and the floor numbers as a digit).