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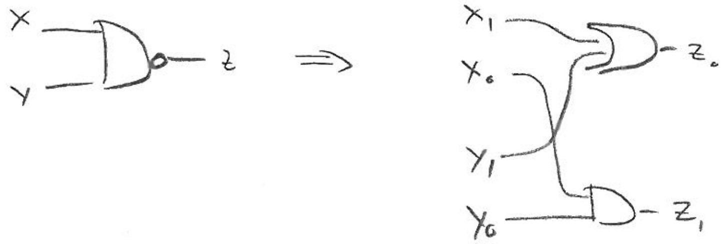
DUAL RAIL LOGIC

SINGLE WIRE CIRCUIT USING NOT, AND, NAND, OR, NOR

$\Rightarrow$ DUAL RAIL REPRESENTATION USING AND, OR
(Maximally 2x as many gates)

NAND



(XOR uses four gates)
works for feed-forward circuits

x_0 : ON $\Rightarrow$ logical „0"

x_1 : ON = „1"

x_0, x_1 : OFF $\Rightarrow$ not yet computed

x_0, x_1 : ON $\Rightarrow$ error

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ARE COMPONENTS DIGITAL?

$$I + G \xrightarrow{k} O + W$$

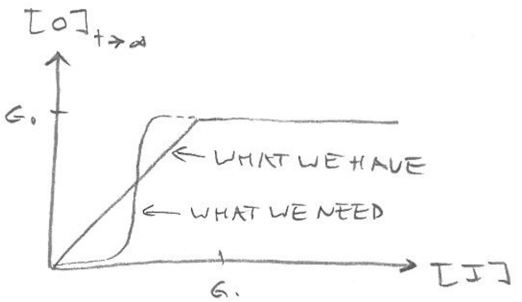
$$\frac{d[G]}{dt} = -k[I][G] = -\frac{d[O]}{dt}, \quad [I(0)] = I_0, \quad [G(0)] = G_0$$

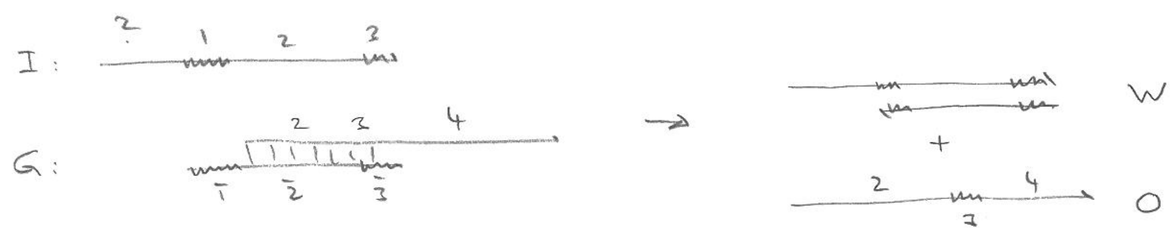
$$\Rightarrow O(t) = G_0\left(1 - \frac{G_0 - I_0}{G_0 - I_0 e^{-k(G_0 - I_0)t}}\right) \qquad G_0 > I_0$$

$$t = 0: \quad O(t) = G_0 - G_0\frac{G_0 - I_0}{G_0 - I_0} = 0 \checkmark$$

$$t \to \infty: \quad O(t) = G_0 - G_0\frac{G_0 - I_0}{G_0} = I_0$$

SKIPPED IN CLASS





$\Rightarrow$ NEED THRESHOLDS + AMPLIFICATION

$G_0 >> I_0$: $x = I_0/G_0 << 1$

$$\underline{O(t)} = G_0\left(1 - \frac{1-x}{1-xe^{-kG_0(1-x)t}}\right) \qquad \text{use } ae^{+x} \cong a(1+x)$$

SERIES EXP.

$$\cong G_0\left(1 - \frac{1-x}{1-x(1+x)e^{-kG_0t}}\right) \qquad \frac{1}{1-xa} \cong 1+xa$$

$$\cong G_0\left(1-(1-x)\left(1+xe^{-kG_0t}\right)\right) \cong G_0\left(1-\left(1-x+xe^{-kG_0t}\right)\right)$$

$$= G_0x\left(1-e^{-kG_0t}\right) = \underline{I_0\left(1-e^{-kG_0t}\right)} \qquad \text{(only slow result!)}$$

similar to unimolecular!

$G_0 \to I_0$: $\frac{G_0 - I_0}{G_0} << 1$

$$\underline{O(t)} = G_0 - \frac{G_0-I_0}{G_0-I_0\left(1-k(G_0-I_0)t\right)} = G_0 - \frac{G_0-I_0}{G_0-I_0+kI_0(G_0-I_0)t}$$

$$= G_0\frac{\cancel{G_0-I_0}+kI_0(\cancel{G_0-I_0})t\cancel{-G_0+I_0}}{(\cancel{G_0-I_0})(1+kI_0t)} = G_0\frac{kG_0t}{1+kG_0t}$$

$$= \underline{G_0\left(1-\frac{1}{1+kG_0t}\right)}$$

same expression as found for $G_0 = I_0$.

$I + G \xrightarrow{k} O$

$I + T \xrightarrow{q} W_2$

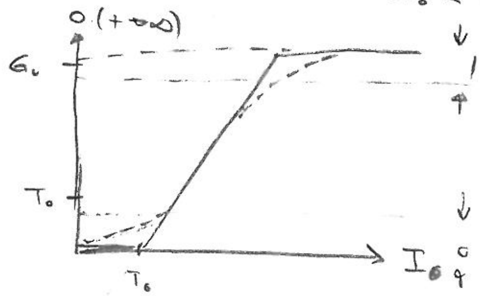
$k \gg q$

$T_0 = G_0/5$

CASE 1: $I_0 < T_0$

CASE 2: $I_0 > G_0 + T_0$

CASE 3: $T_0 < I_0 < G_0 + T_0$



T: THRESHOLD

Rate equations:

1) $\frac{dI}{dt} = -kIG - kIT$

2) $\frac{dG}{dt} = -kIG = +\frac{dO}{dt}$

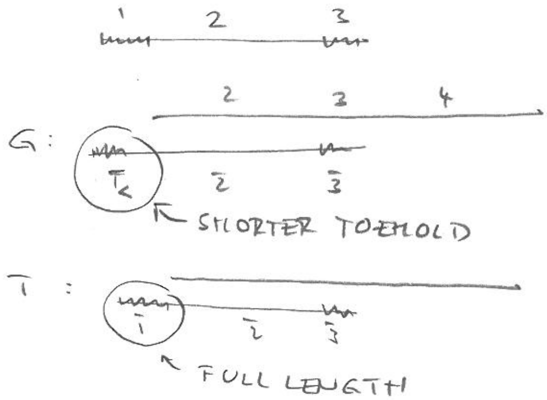
3) $\frac{dT}{dt} = -qIT$

$G_0 = G + O \quad \underbrace{I_0 = I + W \quad T_0 = T + W}_{I_0 - I = T_0 - T}$

$\Rightarrow$ Eq. 3 $\frac{dT}{dt} = -q(I_0 - T_0 + T)T$

THRESHOLDING:

DNA IMPLEMENTATION:



LONGER TOEHOLD $\Rightarrow$ FASTER KINETICS

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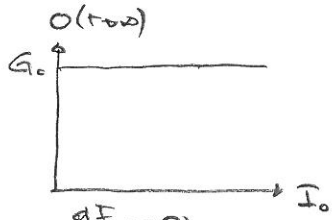
Can we build a better gate?

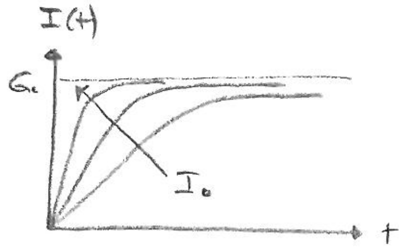
$$I + G \xrightarrow{k} O + I \quad \text{CATALYTIC}$$



$$\frac{dI}{dt} = 0$$

$$\frac{dG}{dt} = -kIG \overset{!}{=} -kI_0 G \Rightarrow G(t) = G_0 e^{-kI_0 t}$$

$$I(t) = G_0\left(1 - e^{-kI_0 t}\right)$$



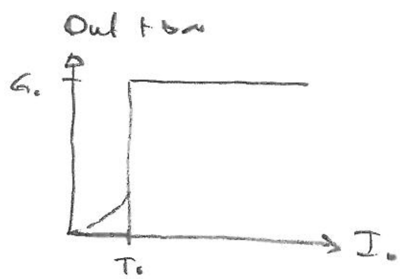
LARGER I_0, FASTER KINETICS!

How about

$$I + G \xrightarrow{k} O + I$$

$$I + T \xrightarrow{q} W$$

If $k \gg q$ and $T_0 < G_0$



$$\frac{dI}{dt} = -qIT$$

$$\frac{dG}{dt} = -kIG = -\frac{dO}{dt}$$

$$\frac{dT}{dt} = -qIT$$

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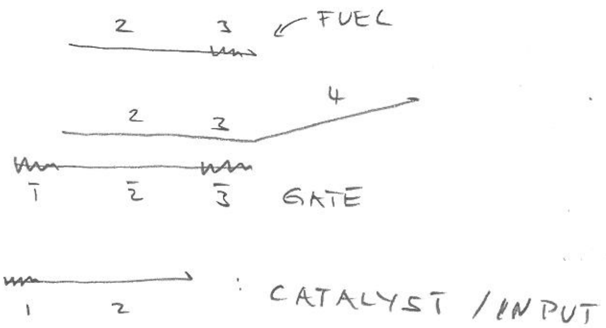
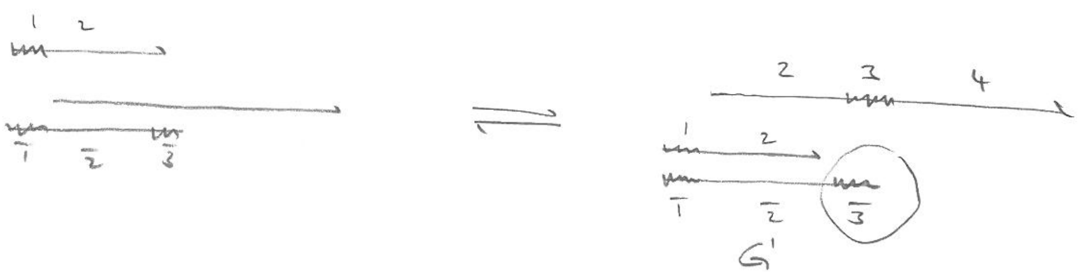
(7) CATALYTIC AMPLIFICATION

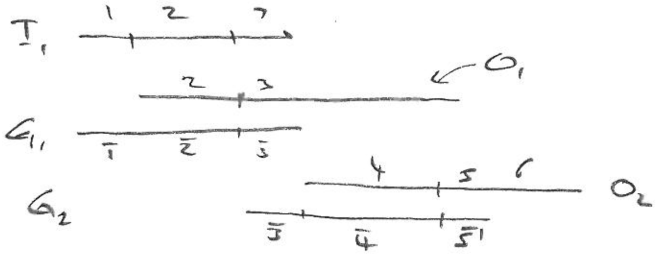


(a) $I + G \rightleftharpoons G' + O$



(b) $G' + F \rightleftharpoons I + W$

=> REPEAT (EACH CYCLE USES 1G, 1F BUT NO C!)



MODEL FOR REACTION CASCADE:

$$I + G_1 \xrightarrow{k_1} O_1$$

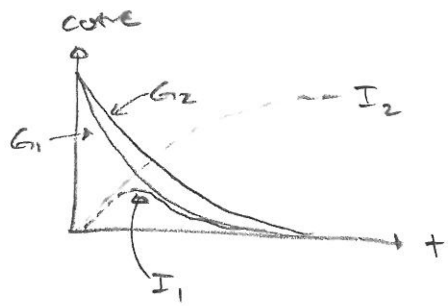
$$O_1 + G_2 \xrightarrow{k} O_2$$

$$\frac{dI}{dt} = -kI_1G_1 = \frac{dG_1}{dt}$$

$$\frac{dO_1}{dt} = +kI_1G_1 - kO_1G_2$$

$$\frac{dG_2}{dt} = -kO_1G_2$$

$$\frac{dO_2}{dt} = +kO_1G_2$$



⇒ speed of multi layered circuits?

⇒ KINETICS as a programming language.