Class Project
Overview

• We want y’all to go do something that:
  • Is exciting (your excitement > our excitement)
  • Uses BlackParrot in some way
  • *Gets completed by the end of the course!!!*
Overview

• Do you have substantial experience writing Verilog?
  • If so, maybe hack on the core!
    • Parametrizable DCACHE size?
    • Optimize single core BP with parameters?
  • Do something cool that we read about!
  • Add CISC instructions that you can run through software!
  • Make BP out-of-order! (mostly a joke)
• Add an FPU!
Examples

- Less experience writing Verilog?
  - Port multi-core benchmarks!
  - Integrate LLVM into the toolchain! (+fancy compiler pass)
  - Do something cool that we read about, or something you’ve read about in your own research!
Logistics

• Teams of two (we’ll *might* have one team of three), working alone is ok, but probably not nearly as fun

• There needs to be a *measurable unit of work* that you can accomplish and demonstrate in two weeks

• *We’ll have part of Monday be dedicated to proposals*
Proposals

• 5 minutes

• Describe what you’re doing

• Describe what your two-week checkpoint is (LO3)

• Tell us why you’ve chosen your project

• Tell us why this will get completed by the end of the course (5-6 weeks from Monday)
Project

• Do something, then:

  • **Talk about it:** we’ll have ~10min presentations at end of the course (last day of classes)

  • **Write about it:** You’ll submit a short paper (4-6p) that goes into more detail than your talk (due during finals week)