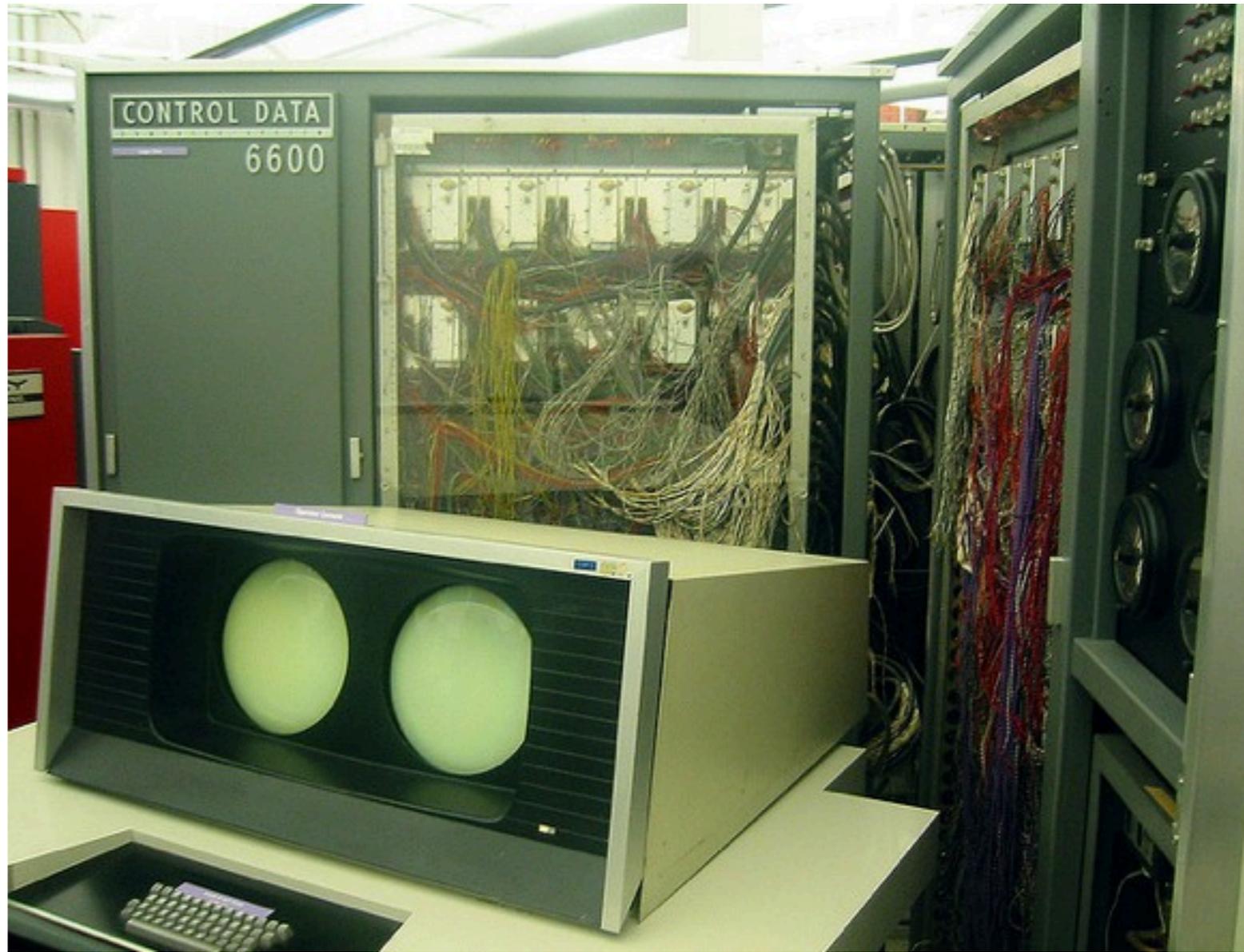
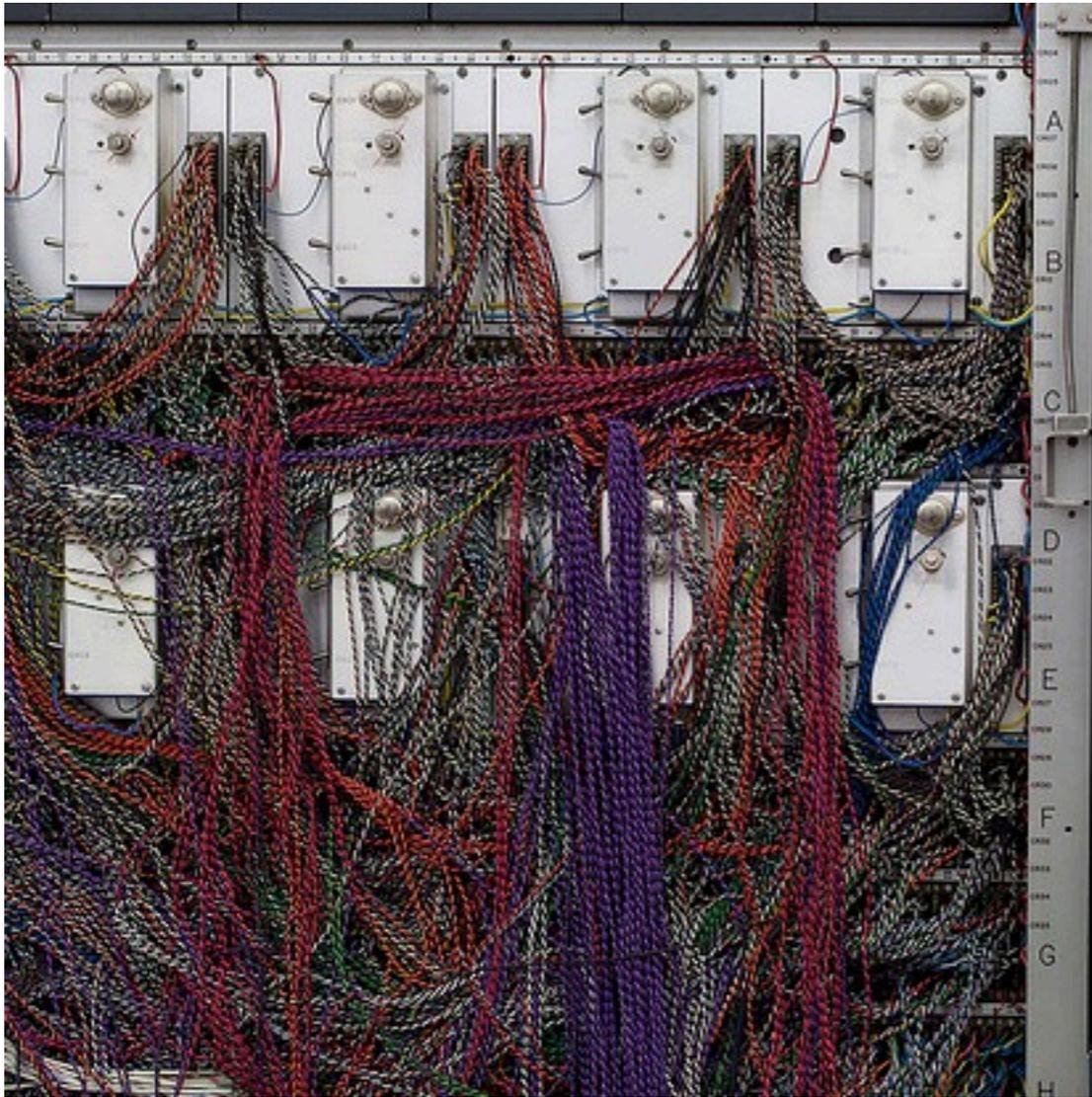
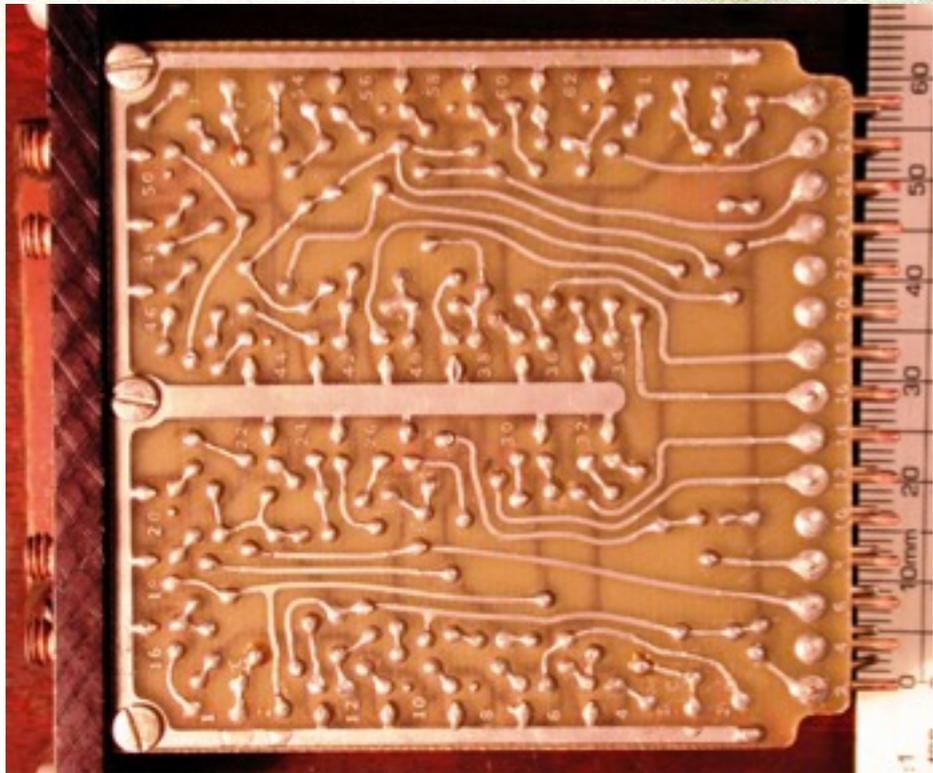
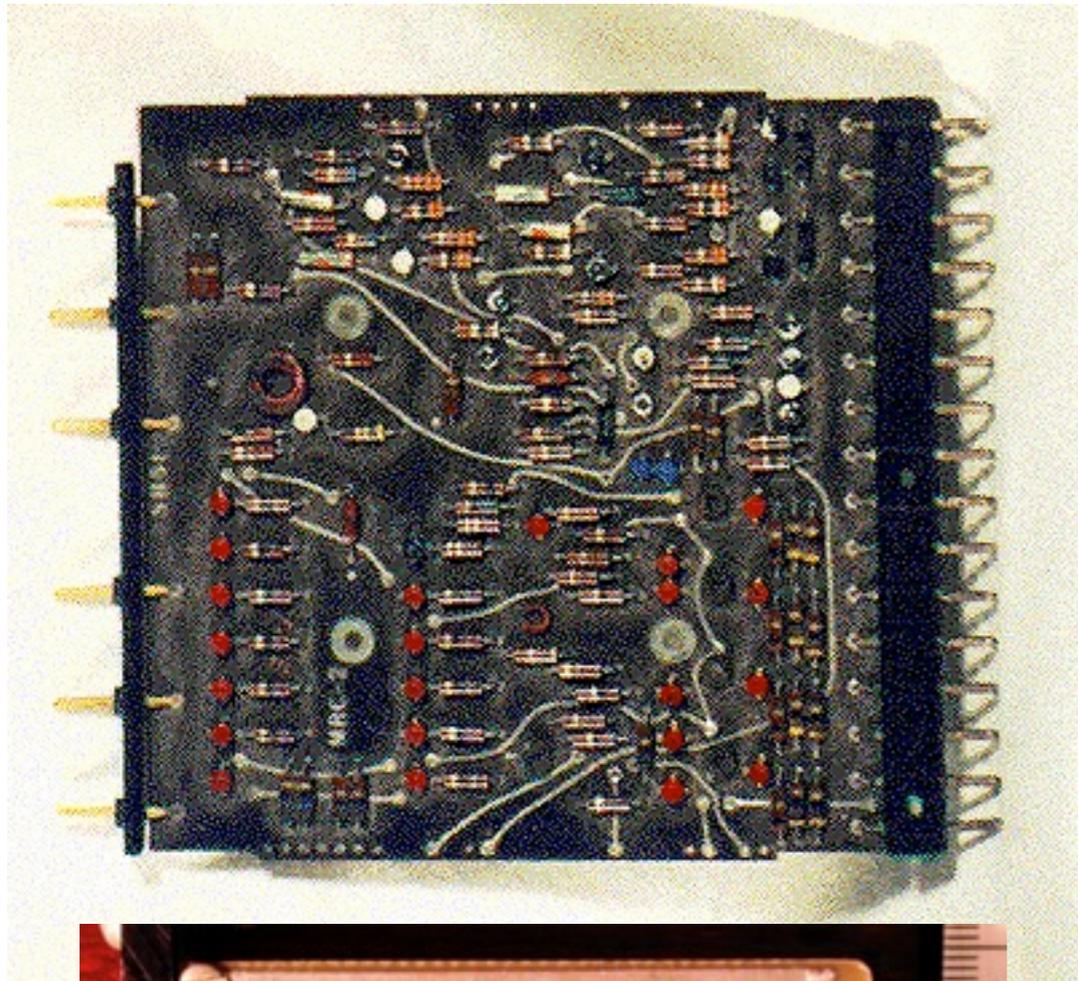


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Lecture 4 - CDC 6600







Why bother with executing out of order?

- Faster (hopefully)
- Execute operations sooner than when they came in program sequence
- An instruction fetched later may not be dependent
- Compiler order \neq critical path order
- Dynamic loop unrolling
- Bypassing long-latency operations, maximize parallelism
- Compilers not up to snuff

Mem->Issue

- Have:
 - Instruction & its bits
- WaitFor:
 - Spot in the scoreboard
- Do
 - Do it! Move instruction to scoreboard

Issue->Dispatch

- WaitFor
 - A functional unit that is free
 - Wait for result register to be free
- Do
 - Assign instruction to functional unit

Dispatch->Execute

- WaitFor
 - Operands to be ready
 - For the execute path to be free
- Do
 - Execute!

Execute -> Complete

- WaitFor
 - Execution to complete
 - Result bus
 - Wait for write-after-read conflicts to resolve
- Do
 - Broadcast result + metadata

Complete

- WaitFor
 - Register write to complete
- Do
 - Erase it
 - Free the functional unit resources

When is scoreboarding successful?

- When computing independent results written to different locations from a variety of functional units

Scoreboard Example

Scoreboard Example

Instruction status

Instruction	j	k
LD F6	34+	R2
LD F2	45+	R3
MULTI F0	F2	F4
SUBD F8	F6	F2
DIVD F10	F0	F6
ADDD F6	F8	F2

Read Executi Write
 operanc complet Result

Issue				
-------	--	--	--	--

Functional unit status

Time	Name
	Integer
	Mult1
	Mult2
	Add
	Divide

Busy Op dest S1 S2 FU for j FU for k Fj? Fk?
 Fi Fj Fk Qj Qk Rj Rk

No								
No								
No								
No								
No								

Register result status

Clock

F0 F2 F4 F6 F8 F10 F12 ... F30

FU

--	--	--	--	--	--	--	--	--

Scoreboard Example Cycle 1

<u>Instruction status</u>				Read	Executic	Write						
Instruction	j	k	Issue	operand	complet	Result						
LD	F6	34+	R2	1								
LD	F2	45+	R3									
MULTI	F0	F2	F4									
SUBD	F8	F6	F2									
DIVD	F10	F0	F6									
ADDD	F6	F8	F2									
<u>Functional unit status</u>				dest	S1	S2	FU for j	FU for k	Fj?	Fk?		
Time	Name	Busy	Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk		
	Integer	Yes	Load	F6		R2				Yes		
	Mult1	No										
	Mult2	No										
	Add	No										
	Divide	No										
<u>Register result status</u>												
Clock	FU	F0	F2	F4	F6	F8	F10	F12	...	F30		
1		Integer										

Scoreboard Example Cycle 2

Instruction status

Instruction	j	k
LD F6	34+	R2
LD F2	45+	R3
MULTI F0	F2	F4
SUBD F8	F6	F2
DIVD F10	F0	F6
ADDD F6	F8	F2

Issue	Read operand	Executic complet	Write Result
1	2		

Functional unit status

Time Name

Busy	Op	dest Fi	S1 Fj	S2 Fk	FU for j Qj	FU for k Qk	Fj? Rj	Fk? Rk
Yes	Load	F6		R2				Yes
No								
No								
No								
No								

Register result status

Clock

2

FU

F0	F2	F4	F6	F8	F10	F12	...	F30
			Integer					

Scoreboard Example Cycle 3

Instruction status

Instruction	j	k	Issue	Read operand	Executic complet	Write Result
LD	F6	34+	R2	1	2	3
LD	F2	45+	R3			
MULTI	F0	F2	F4			
SUBD	F8	F6	F2			
DIVD	F10	F0	F6			
ADDD	F6	F8	F2			

Functional unit status

Time Name

Busy	Op	dest	S1	S2	FU for j	FU for k	Fj?	Fk?
		Fi	Fj	Fk	Qj	Qk	Rj	Rk
Yes	Load	F6		R2				Yes
No								
No								
No								
No								

Register result status

Clock

3

FU

F0	F2	F4	F6	F8	F10	F12	...	F30
Integer								

Scoreboard Example Cycle 4

Instruction status

Instruction	j	k	Issue	Read operand	Executic complet	Write Result
			1	2	3	4
LD F6	34+	R2				
LD F2	45+	R3				
MULTI F0	F2	F4				
SUBD F8	F6	F2				
DIVD F10	F0	F6				
ADDD F6	F8	F2				

Functional unit status

Time Name

Busy	Op	dest	S1	S2	FU for j	FU for k	Fj?	Fk?
		Fi	Fj	Fk	Qj	Qk	Rj	Rk
Yes	Load	F6		R2				Yes
No								
No								
No								
No								

Register result status

Clock

4

FU

F0	F2	F4	F6	F8	F10	F12	...	F30
Integer								

Scoreboard Example Cycle 5

Instruction status

Instruction	j	k	Issue	Read operand	Executic complet	Write Result	
LD	F6	34+	R2	1	2	3	4
LD	F2	45+	R3	5			
MULTI	F0	F4					
SUBD	F8	F6	F2				
DIVD	F10	F0	F6				
ADDD	F6	F8	F2				

Functional unit status

Time Name

Integer
Mult1
Mult2
Add
Divide

Busy	Op	dest Fi	S1 Fj	S2 Fk	FU for j Qj	FU for k Qk	Fj? Rj	Fk? Rk
Yes	Load	F2		R3				Yes
No								
No								
No								
No								

Register result status

Clock

5

FU

F0	F2	F4	F6	F8	F10	F12	...	F30
	Integer							

Scoreboard Example Cycle 6

<u>Instruction status</u>				Read	Executic	Write					
Instruction	j	k	Issue	operand	complet	Result					
LD	F6	34+	R2	1	2	3	4				
LD	F2	45+	R3	5	6						
MULTI	F0	F2	F4	6							
SUBD	F8	F6	F2								
DIVD	F10	F0	F6								
ADDD	F6	F8	F2								

<u>Functional unit status</u>		Busy	Op	dest	S1	S2	FU for j	FU for k	Fj?	Fk?
Time	Name			Fi	Fj	Fk	Qj	Qk	Rj	Rk
	Integer	Yes	Load	F2		R3				Yes
	Mult1	Yes	Mult	F0	F2	F4	Integer		No	Yes
	Mult2	No								
	Add	No								
	Divide	No								

<u>Register result status</u>		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock										
6	FU	Mult1	Integer							

Scoreboard Example Cycle 7

Instruction status

Instruction	j	k	Issue	Read operand	Executic complet	Write Result	
LD	F6	34+	R2	1	2	3	4
LD	F2	45+	R3	5	6	7	
MULTI	F0	F2	F4	6			
SUBD	F8	F6	F2	7			
DIVD	F10	F0	F6				
ADDD	F6	F8	F2				

Functional unit status

Time Name

Busy	Op	dest Fi	S1 Fj	S2 Fk	FU for j Qj	FU for k Qk	Fj? Rj	Fk? Rk
Yes	Load	F2		R3				Yes
Yes	Mult	F0	F2	F4	Integer		No	Yes
No								
Yes	Sub	F8	F6	F2		Integer	Yes	No
No								

Register result status

Clock

7

FU

F0	F2	F4	F6	F8	F10	F12	...	F30
Mult1	Integer			Add				

Scoreboard Example Cycle 8a

Instruction status

Instruction	j	k	Issue	Read operand	Executic complet	Write Result
LD	F6	34+	R2	1	2	3 4
LD	F2	45+	R3	5	6	7
MULTI	F0	F2	F4	6		
SUBD	F8	F6	F2	7		
DIVD	F10	F0	F6	8		
ADDD	F6	F8	F2			

Functional unit status

Time Name

Busy	Op	dest Fi	S1 Fj	S2 Fk	FU for j Qj	FU for k Qk	Fj? Rj	Fk? Rk
Yes	Load	F2		R3				Yes
Yes	Mult	F0	F2	F4	Integer		No	Yes
No								
Yes	Sub	F8	F6	F2		Integer	Yes	No
Yes	Div	F10	F0	F6	Mult1		No	Yes

Register result status

Clock

8

FU

F0	F2	F4	F6	F8	F10	F12	...	F30
Mult1	Integer			Add	Divide			

Scoreboard Example Cycle 8b

Instruction status

Instruction	j	k	Issue	Read operand	Executic complet	Write Result
LD	F6	34+	R2	1	2	3 4
LD	F2	45+	R3	5	6	7 8
MULTI	F0	F2	F4	6		
SUBD	F8	F6	F2	7		
DIVD	F10	F0	F6	8		
ADDD	F6	F8	F2			

Functional unit status

Time Name

Busy	Op	dest Fi	S1 Fj	S2 Fk	FU for j Qj	FU for k Qk	Fj? Rj	Fk? Rk
No								
Yes	Mult	F0	F2	F4			Yes	Yes
No								
Yes	Sub	F8	F6	F2			Yes	Yes
Yes	Div	F10	F0	F6	Mult1		No	Yes

Register result status

Clock

8

FU

F0	F2	F4	F6	F8	F10	F12	...	F30
			Mult1		Add	Divide		

Scoreboard Example Cycle 9

Instruction status

Instruction	j	k	Issue	Read operand	Executic complet	Write Result
LD F6	34+	R2	1	2	3	4
LD F2	45+	R3	5	6	7	8
MULTI F0	F2	F4	6	9		
SUBD F8	F6	F2	7	9		
DIVD F10	F0	F6	8			
ADDD F6	F8	F2				

Functional unit status

Time Name

Integer
10 Mult1
Mult2
2 Add
Divide

Busy	Op	dest Fi	S1 Fj	S2 Fk	FU for j Qj	FU for k Qk	Fj? Rj	Fk? Rk
No								
Yes	Mult	F0	F2	F4			Yes	Yes
No								
Yes	Sub	F8	F6	F2			Yes	Yes
Yes	Div	F10	F0	F6	Mult1		No	Yes

Register result status

Clock

9

FU

F0	F2	F4	F6	F8	F10	F12	...	F30
			Mult1		Add	Divide		

Scoreboard Example Cycle 11

<u>Instruction status</u>				Read	Executic	Write					
Instruction	j	k	Issue	operand	complet	Result					
LD	F6	34+	R2	1	2	3	4				
LD	F2	45+	R3	5	6	7	8				
MULTI	F0	F2	F4	6	9						
SUBD	F8	F6	F2	7	9	11					
DIVD	F10	F0	F6	8							
ADDD	F6	F8	F2								

<u>Functional unit status</u>		Busy	Op	dest	S1	S2	FU for j	FU for k	Fj?	Fk?
Time	Name			Fi	Fj	Fk	Qj	Qk	Rj	Rk
	Integer	No								
8	Mult1	Yes	Mult	F0	F2	F4			Yes	Yes
	Mult2	No								
0	Add	Yes	Sub	F8	F6	F2			Yes	Yes
	Divide	Yes	Div	F10	F0	F6	Mult1		No	Yes

<u>Register result status</u>		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock										
11	FU	Mult1				Add	Divide			

Scoreboard Example Cycle 12

Instruction status

Instruction	j	k	Issue	Read operand	Executic complet	Write Result
LD F6	34+	R2	1	2	3	4
LD F2	45+	R3	5	6	7	8
MULTI F0	F2	F4	6	9		
SUBD F8	F6	F2	7	9	11	12
DIVD F10	F0	F6	8			
ADDD F6	F8	F2				

Functional unit status

Time Name

Integer
7 Mult1
Mult2
Add
Divide

Busy	Op	dest Fi	S1 Fj	S2 Fk	FU for j Qj	FU for k Qk	Fj? Rj	Fk? Rk
No								
Yes	Mult	F0	F2	F4			Yes	Yes
No								
No								
Yes	Div	F10	F0	F6	Mult1		No	Yes

Register result status

Clock

12

FU

F0	F2	F4	F6	F8	F10	F12	...	F30
Mult1						Divide		

Scoreboard Example Cycle 14

<u>Instruction status</u>				Read	Executic	Write
Instruction	j	k	Issue	operand	complet	Result
LD	F6	34+	1	2	3	4
LD	F2	45+	5	6	7	8
MULTI	F0	F4	6	9		
SUBD	F8	F2	7	9	11	12
DIVD	F10	F6	8			
ADDD	F6	F2	13	14		

<u>Functional unit status</u>		Busy	Op	dest	S1	S2	FU for j	FU for k	Fj?	Fk?
Time	Name			Fi	Fj	Fk	Qj	Qk	Rj	Rk
	Integer	No								
5	Mult1	Yes	Mult	F0	F2	F4			Yes	Yes
	Mult2	No								
2	Add	Yes	Add	F6	F8	F2			Yes	Yes
	Divide	Yes	Div	F10	F0	F6	Mult1		No	Yes

<u>Register result status</u>		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock	FU	Mult1			Add		Divide			
14										

Scoreboard Example Cycle 15

Instruction status

Instruction	j	k	Issue	Read operand	Executic complet	Write Result
LD	F6	34+	R2	1	2	3 4
LD	F2	45+	R3	5	6	7 8
MULTI	F0	F2	F4	6	9	
SUBD	F8	F6	F2	7	9	11 12
DIVD	F10	F0	F6	8		
ADDD	F6	F8	F2	13	14	

Functional unit status

Time Name

Integer
4 Mult1
Mult2
1 Add
Divide

Busy	Op	dest Fi	S1 Fj	S2 Fk	FU for j Qj	FU for k Qk	Fj? Rj	Fk? Rk
No								
Yes	Mult	F0	F2	F4			Yes	Yes
No								
Yes	Add	F6	F8	F2			Yes	Yes
Yes	Div	F10	F0	F6	Mult1		No	Yes

Register result status

Clock

15

FU

F0	F2	F4	F6	F8	F10	F12	...	F30
Mult1			Add		Divide			

Scoreboard Example Cycle 16

<u>Instruction status</u>				Read	Executic	Write					
Instruction	j	k	Issue	operand	complet	Result					
LD	F6	34+	R2	1	2	3	4				
LD	F2	45+	R3	5	6	7	8				
MULTI	F0	F2	F4	6	9						
SUBD	F8	F6	F2	7	9	11	12				
DIVD	F10	F0	F6	8							
ADDD	F6	F8	F2	13	14	16					

<u>Functional unit status</u>			dest	S1	S2	FU for j	FU for k	Fj?	Fk?	
Time	Name	Busy	Op	Fi	Fj	Fk	Qj	Qk	Rj	Rk
	Integer	No								
3	Mult1	Yes	Mult	F0	F2	F4			Yes	Yes
	Mult2	No								
0	Add	Yes	Add	F6	F8	F2			Yes	Yes
	Divide	Yes	Div	F10	F0	F6	Mult1		No	Yes

<u>Register result status</u>		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock	FU	Mult1			Add		Divide			
16										

Scoreboard Example Cycle 17

Instruction status

Instruction	j	k	Issue	Read operand	Executic complet	Write Result
LD	F6	34+	R2	1	2	3 4
LD	F2	45+	R3	5	6	7 8
MULTI	F0	F2	F4	6	9	
SUBD	F8	F6	F2	7	9	11 12
DIVD	F10	F0	F6	8		
ADDD	F6	F8	F2	13	14	16

Functional unit status

Time Name

Integer
2 Mult1
Mult2
Add
Divide

Busy	Op	dest Fi	S1 Fj	S2 Fk	FU for j Qj	FU for k Qk	Fj? Rj	Fk? Rk
No								
Yes	Mult	F0	F2	F4			Yes	Yes
No								
Yes	Add	F6	F8	F2			Yes	Yes
Yes	Div	F10	F0	F6	Mult1		No	Yes

Register result status

Clock

17

FU

F0	F2	F4	F6	F8	F10	F12	...	F30
Mult1			Add		Divide			

Scoreboard Example Cycle 18

Instruction status				Read	Executic	Write
Instruction	j	k	Issue	operand	complet	Result
LD	F6	34+	1	2	3	4
LD	F2	45+	5	6	7	8
MULTI	F0	F4	6	9		
SUBD	F8	F2	7	9	11	12
DIVD	F10	F6	8			
ADDD	F6	F8	13	14	16	

Functional unit status		Busy	Op	dest	S1	S2	FU for j	FU for k	Fj?	Fk?
Time	Name			Fi	Fj	Fk	Qj	Qk	Rj	Rk
	Integer	No								
1	Mult1	Yes	Mult	F0	F2	F4			Yes	Yes
	Mult2	No								
	Add	Yes	Add	F6	F8	F2			Yes	Yes
	Divide	Yes	Div	F10	F0	F6	Mult1		No	Yes

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock	FU	Mult1			Add		Divide			
18										

Scoreboard Example Cycle 19

<u>Instruction status</u>				Read	Executic	Write					
Instruction	j	k	Issue	operand	complet	Result					
LD	F6	34+	R2	1	2	3	4				
LD	F2	45+	R3	5	6	7	8				
MULTI	F0	F2	F4	6	9	19					
SUBD	F8	F6	F2	7	9	11	12				
DIVD	F10	F0	F6	8							
ADDD	F6	F8	F2	13	14	16					

<u>Functional unit status</u>		Busy	Op	dest	S1	S2	FU for j	FU for k	Fj?	Fk?
Time	Name			Fi	Fj	Fk	Qj	Qk	Rj	Rk
	Integer	No								
0	Mult1	Yes	Mult	F0	F2	F4			Yes	Yes
	Mult2	No								
	Add	Yes	Add	F6	F8	F2			Yes	Yes
	Divide	Yes	Div	F10	F0	F6	Mult1		No	Yes

<u>Register result status</u>		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock										
19	FU	Mult1			Add		Divide			

Scoreboard Example Cycle 20

Instruction status

Instruction	j	k	Issue	Read operand	Executic complet	Write Result
LD	F6	34+	R2	1	2	3 4
LD	F2	45+	R3	5	6	7 8
MULTI	F0	F2	F4	6	9	19 20
SUBD	F8	F6	F2	7	9	11 12
DIVD	F10	F0	F6	8		
ADDD	F6	F8	F2	13	14	16

Functional unit status

Time	Name	Busy	Op	dest Fi	S1 Fj	S2 Fk	FU for j Qj	FU for k Qk	Fj? Rj	Fk? Rk
	Integer	No								
	Mult1	No								
	Mult2	No								
	Add	Yes	Add	F6	F8	F2			Yes	Yes
	Divide	Yes	Div	F10	F0	F6			Yes	Yes

Register result status

Clock	F0	F2	F4	F6	F8	F10	F12	...	F30
20				Add		Divide			

Scoreboard Example Cycle 21

Instruction status				Read	Executic	Write					
Instruction	j	k	Issue	operand	complet	Result					
LD	F6	34+	R2	1	2	3	4				
LD	F2	45+	R3	5	6	7	8				
MULTI	F0	F2	F4	6	9	19	20				
SUBD	F8	F6	F2	7	9	11	12				
DIVD	F10	F0	F6	8	21						
ADDD	F6	F8	F2	13	14	16					

Functional unit status		dest	S1	S2	FU for j	FU for k	Fj?	Fk?
Time	Name	Busy	Op	Fi	Fj	Fk	Qj	Qk
	Integer	No						
	Mult1	No						
	Mult2	No						
	Add	Yes	Add	F6	F8	F2		
	Divide	Yes	Div	F10	F0	F6		
							Yes	Yes
							Yes	Yes

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock	FU				Add		Divide			
21										

Scoreboard Example Cycle 22

<u>Instruction status</u>				Read	Executic	Write					
Instruction	j	k	Issue	operand	complet	Result					
LD	F6	34+	R2	1	2	3	4				
LD	F2	45+	R3	5	6	7	8				
MULTI	F0	F2	F4	6	9	19	20				
SUBD	F8	F6	F2	7	9	11	12				
DIVD	F10	F0	F6	8	21						
ADDD	F6	F8	F2	13	14	16	22				

<u>Functional unit status</u>		Busy	Op	dest	S1	S2	FU for j	FU for k	Fj?	Fk?
Time	Name			Fi	Fj	Fk	Qj	Qk	Rj	Rk
	Integer	No								
	Mult1	No								
	Mult2	No								
	Add	No								
40	Divide	Yes	Div	F10	F0	F6			Yes	Yes

<u>Register result status</u>		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock	FU						Divide			
22										

Scoreboard Example Cycle 62

Instruction status				Read	Executic	Write	
Instruction	j	k	Issue	operand	complet	Result	
LD	F6	34+	R2	1	2	3	4
LD	F2	45+	R3	5	6	7	8
MULT	F0	F2	F4	6	9	19	20
SUBD	F8	F6	F2	7	9	11	12
DIVD	F10	F0	F6	8	21	61	62
ADDD	F6	F8	F2	13	14	16	22

Functional unit status		Busy	Op	dest	S1	S2	FU for j	FU for k	Fj?	Fk?
Time	Name			Fi	Fj	Fk	Qj	Qk	Rj	Rk
	Integer	No								
	Mult1	No								
	Mult2	No								
	Add	No								
	0 Divide	No								

Register result status		F0	F2	F4	F6	F8	F10	F12	...	F30
Clock										
62	FU									

What are the “I/O” “processors”?

- FGMT processors on the 6600
- Uniform instruction set for I/O devices
- Why context switch main memory?
 - This is pre-virtual memory

What is the FIFO instruction stack?

- A very primitive instruction cache
- 8, 60-bit words, up to 32 instructions
- optimized for back-edges

Your questions

- Precise exceptions?
- How much ILP/dataflow study before this?
- How much influence?
- When did memory get slower than computation?
- Major cycle?
- Why 10 control processors?
- What sort of performance improvement was had?
- Why is WAW not immediately resolvable?
- How much overhead is scoreboarding?
- Interrupts?
- Anyone still use this?
- Is 2% contention to be believed?
- Why only communicate via memory?
- Is this truly OoO?
- What about memory dependencies?
- Cost of the broadcast result busses?
- Relationship to Stetch? How to pipeline?
- Relationship between control processors and DMA?
- How much software actually ran on the CPs?
- How does scoreboarding work with timeslicing?
- Is there a place for physical registers in a scoreboarding machine?