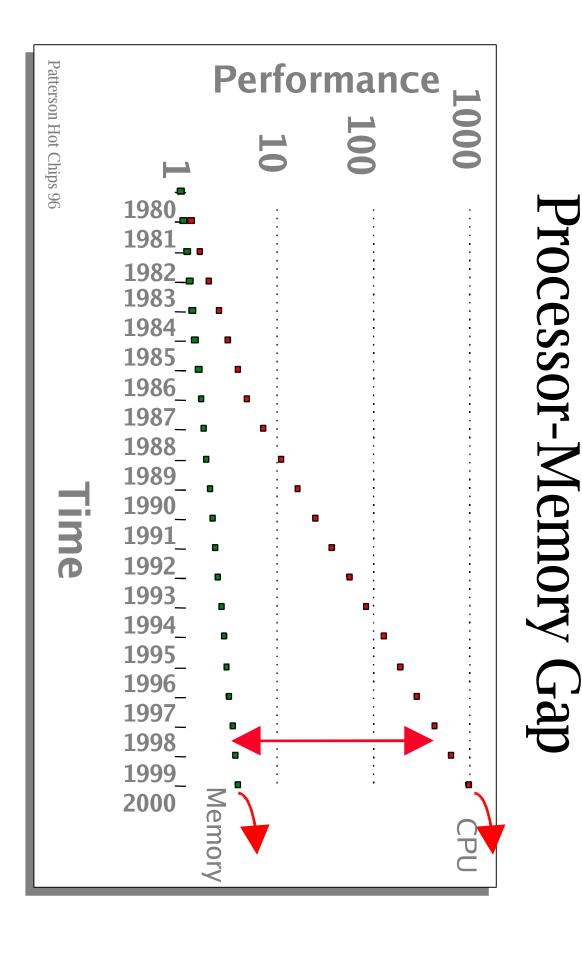
What / Why is memory?

- What
 - Preservation of state
 - Place(n) to place(v) your data
 - Communication mechanism
 - Separates computers from PDA
- Why
 - Time-space trade off

What is the difference between a register and memory?

• Memory gives us indirection



What is the memory hierarchy and why?

- What
 - From disk to registers
 - Registers
 - Level 1 cache
 - Level 2 cache
 - Level 3 in some systems
 - DRAM
 - Disk
 - Diskarray / removable device / Web storage
- Why
 - Time econmic tradeoff

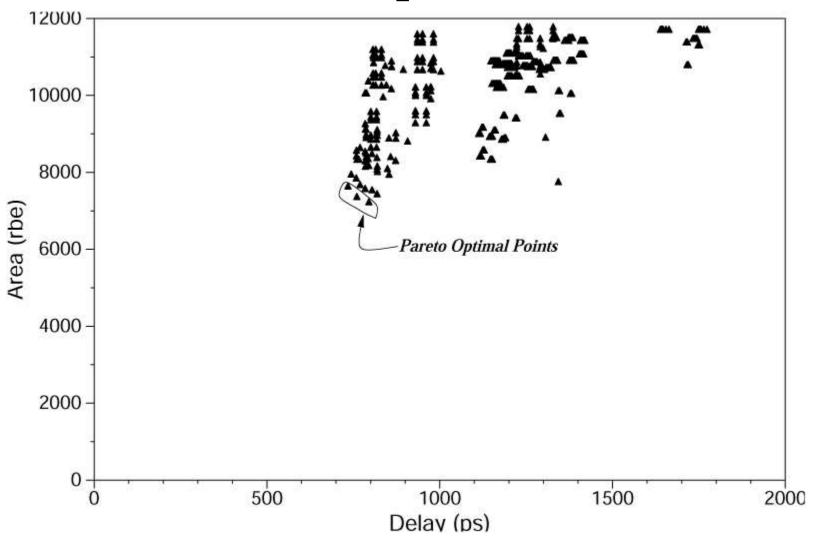
A Cache is a bet...

- What do you lose?
 - \$
 - Look ahead grabbing more data than needed
 - Increased worst-case
- What can you win?
 - Speed in the common case

Stream buffers – implicit prefetching

- Acquire next n lines speculatively
- Prefefch around last cache line
 - Next n cache lines
 - Stride prefetching
 - Markov model prefetching
- Multiple stream buffers

Cache size/speed tradeoff



Where are we going from here?

Problems

- Smoother degradation L1/l2/l3/l?

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Solutions

- Faster memory technology
- Compiler/programming prefetching
- Cache conscious algorithms
- Better prefetching algorithms
 - Fuzzy logic / adaptive

- for(i=0; i<= assoc; i++)
 - a[i*huge#]++

(swiped from Luna)

Don't Need to Pay Much for Your Miss (II) - Lockup-free Instruction Fetch/Prefetch

```
if (send-to-CPU)
if (catch-hit)
   get-from-cache
                                                           send to CPU;
else if (catch-miss){
                                                  if (!totally written || !MSHR obsolete){
   Judge the miss states from MSHR (in-
                                                           if (input-stack full)
   input-stack indicator, partial write codes,
                                                                     FIFO remove one:
   valid indicator);
                                                           write to input-stack;
   if (totally written)
                                                           set MSHR.in-input-stack;
         read from cache;
   else if (in-input-stack)
                                                  write to catch and set MSHR.partial-
         read from input stack;
                                                  write-code
   else if (partially written || already-asked-
                                                  if (written || obsolete MSHR)
   for)
                                                           MSHR_num-of-words-
         by-pass;
                                                  processed++;
   else{
                                                  if (MSHR.num-of-words processed
         initiate MSHR;
                                                  overflow)
         when data available do 1, 2, 3
                                                           clear MSHR.valid-indicator;
   parallely; }
```