Computer-Aided Reasoning for Software

Solver-Aided Languages

courses.cs.washington.edu/courses/cse507/18sp/

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Today

Last lecture

• Program synthesis

Today

Solver-aided languages

Announcements

- Next Wednesday: guest lecture by James Bornholt
- Project presentations next Friday in class
 - 13 min per team: 10 min presentation + 3 min questions
- Project reports and prototypes due next Friday at 11:00pm

How to build your own solver-aided tool



The classic (hard) way to build a tool

What is hard about building a solver-aided tool?

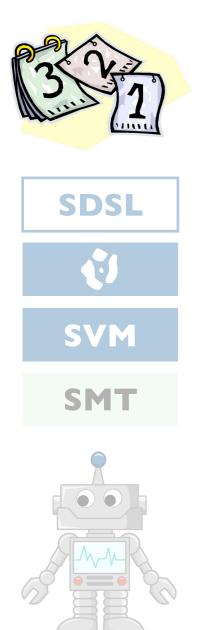
An easier way: tools as languages How to build tools by stacking layers of languages.

Behind the scenes: symbolic virtual machine How Rosette works so you don't have to.

A last look: a few recent applications

Cool tools built with Rosette!

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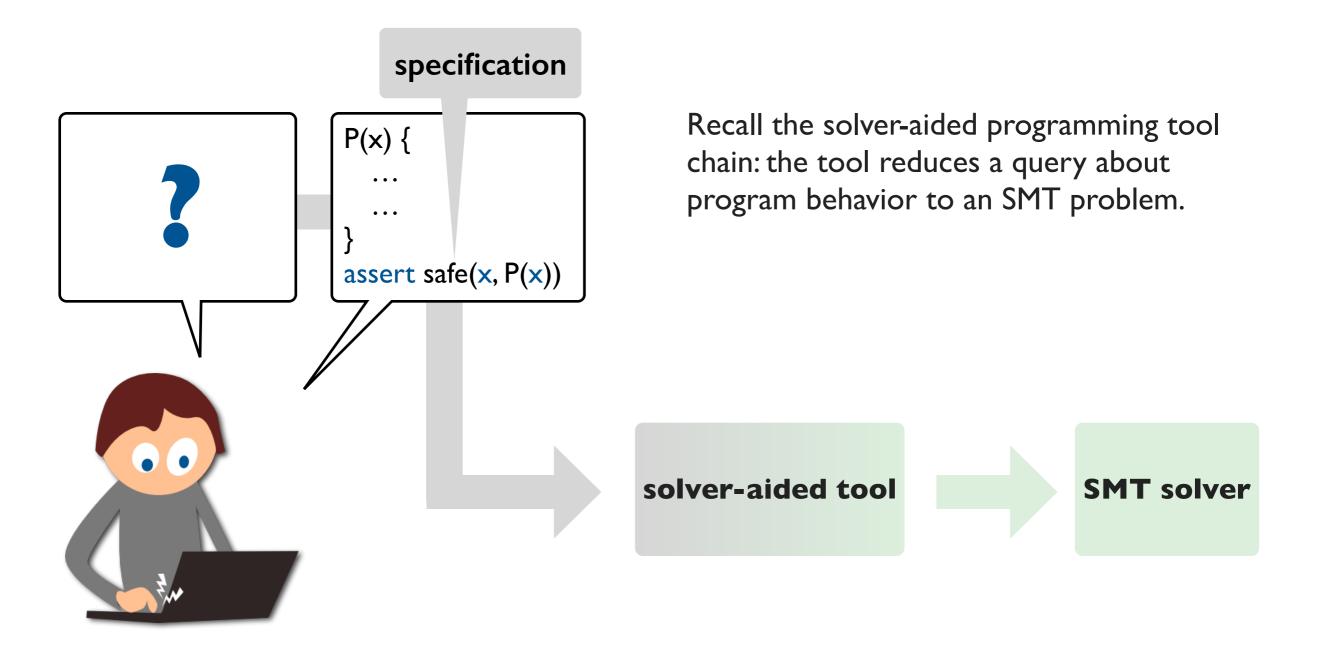
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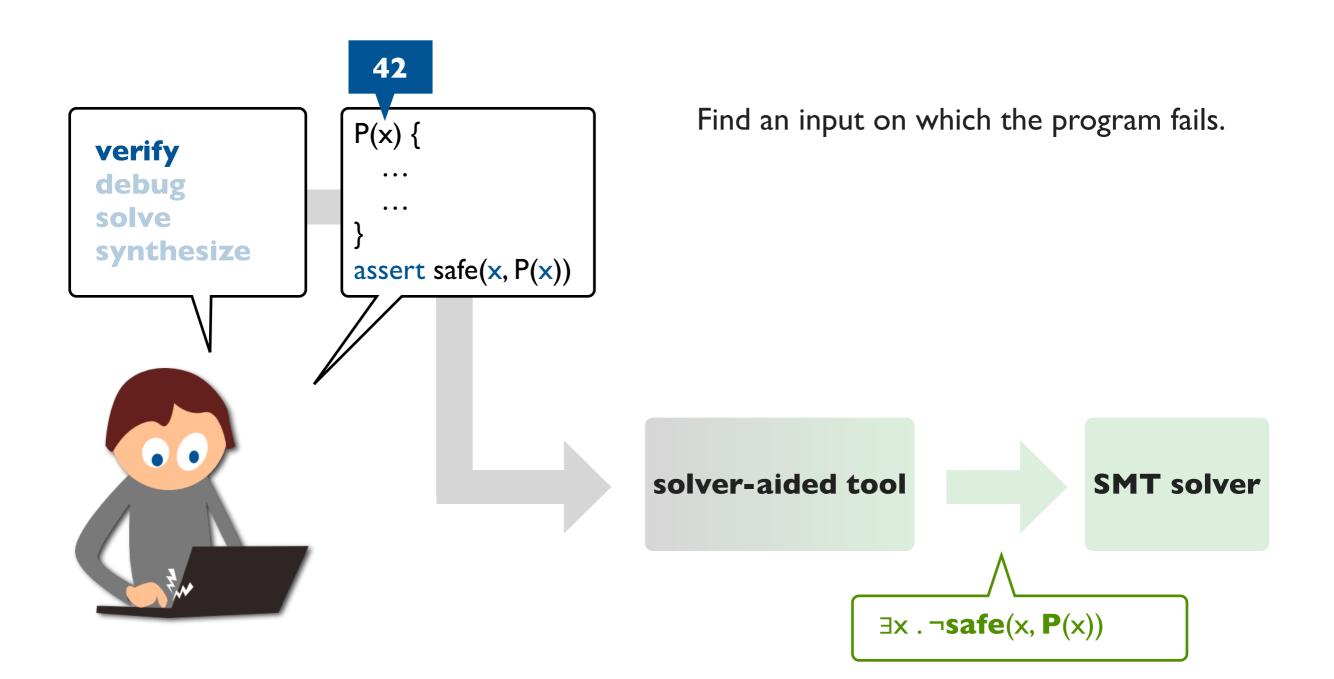
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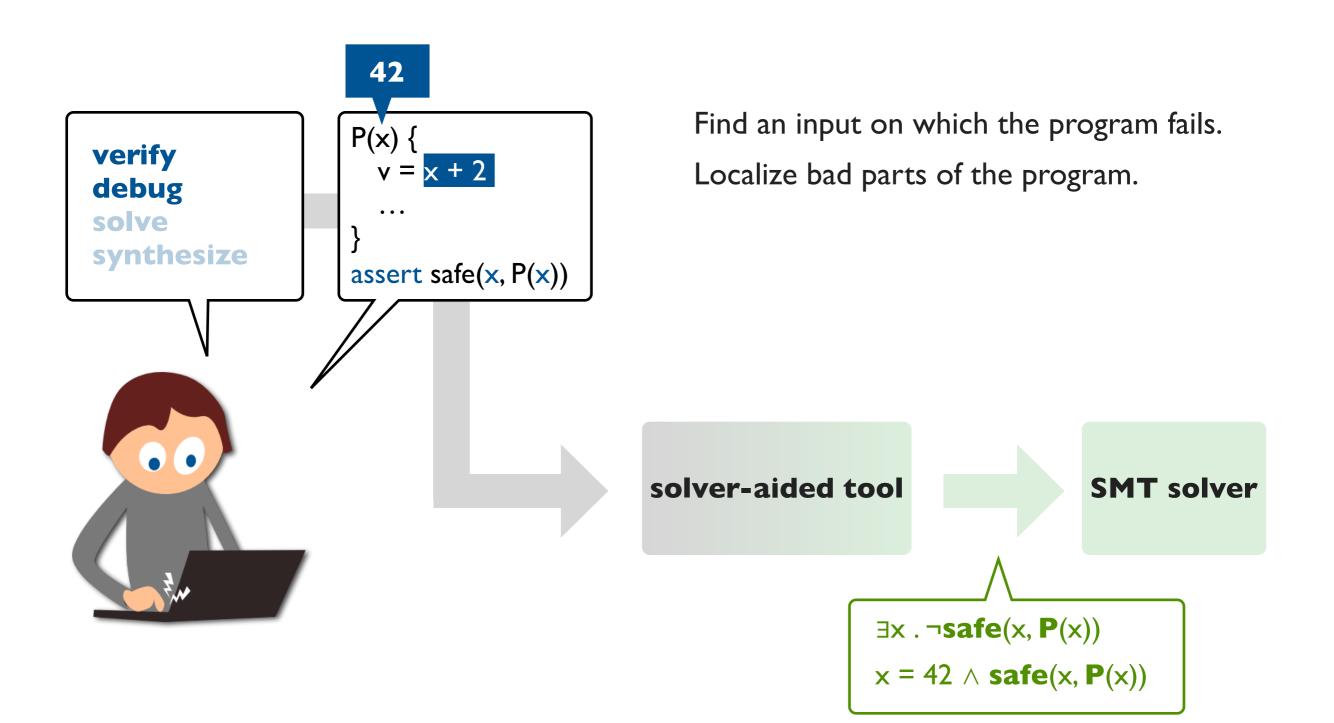




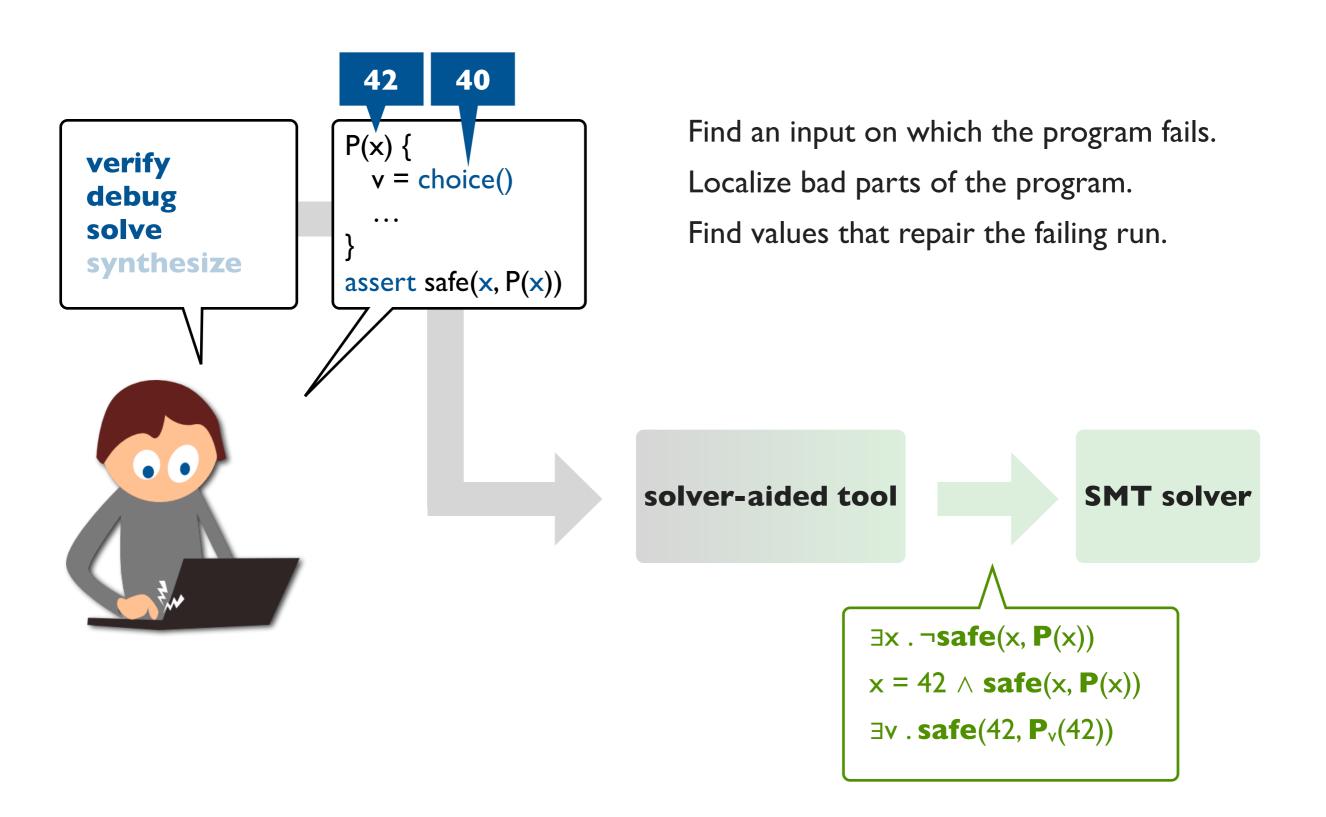




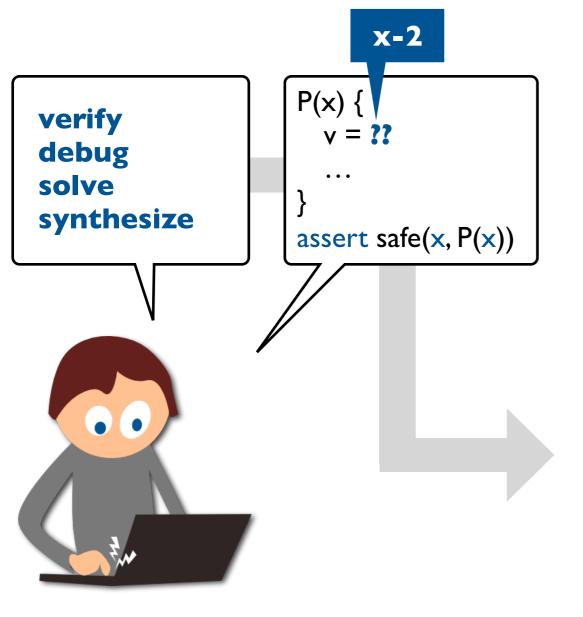




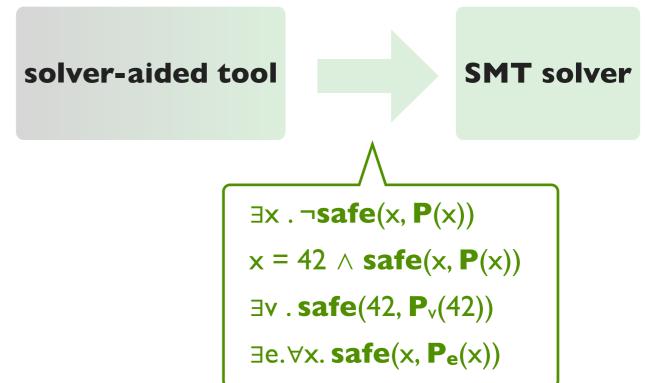




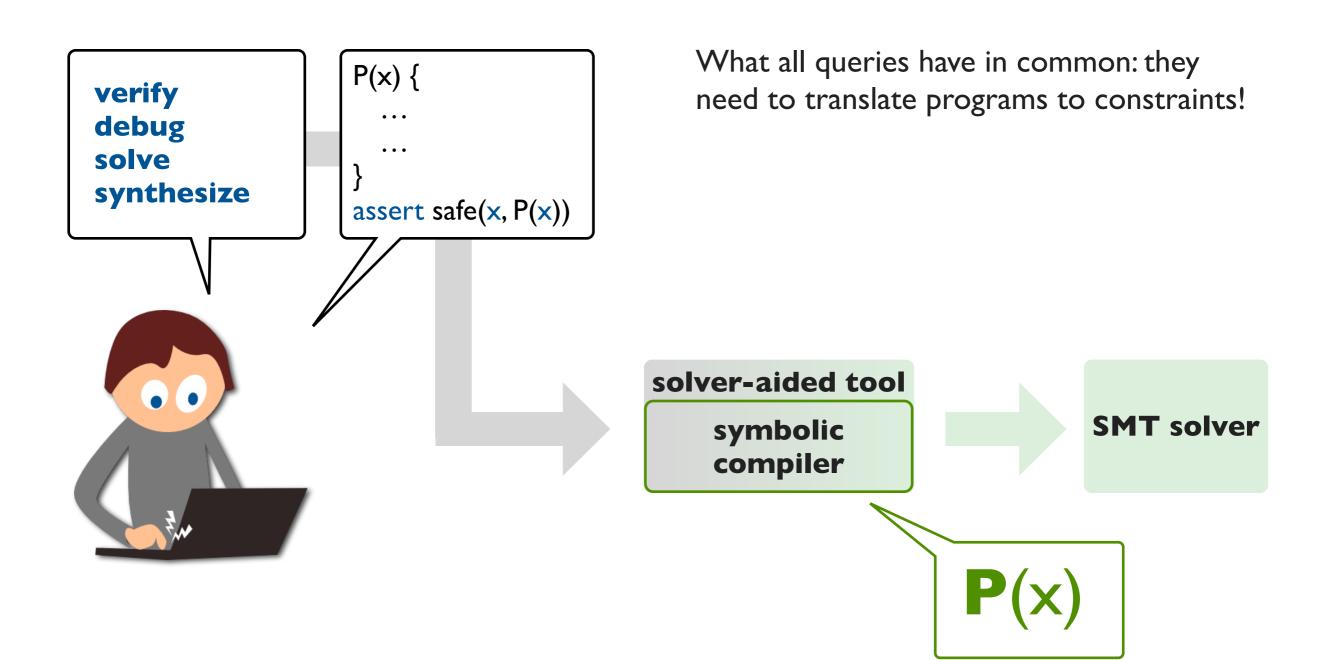


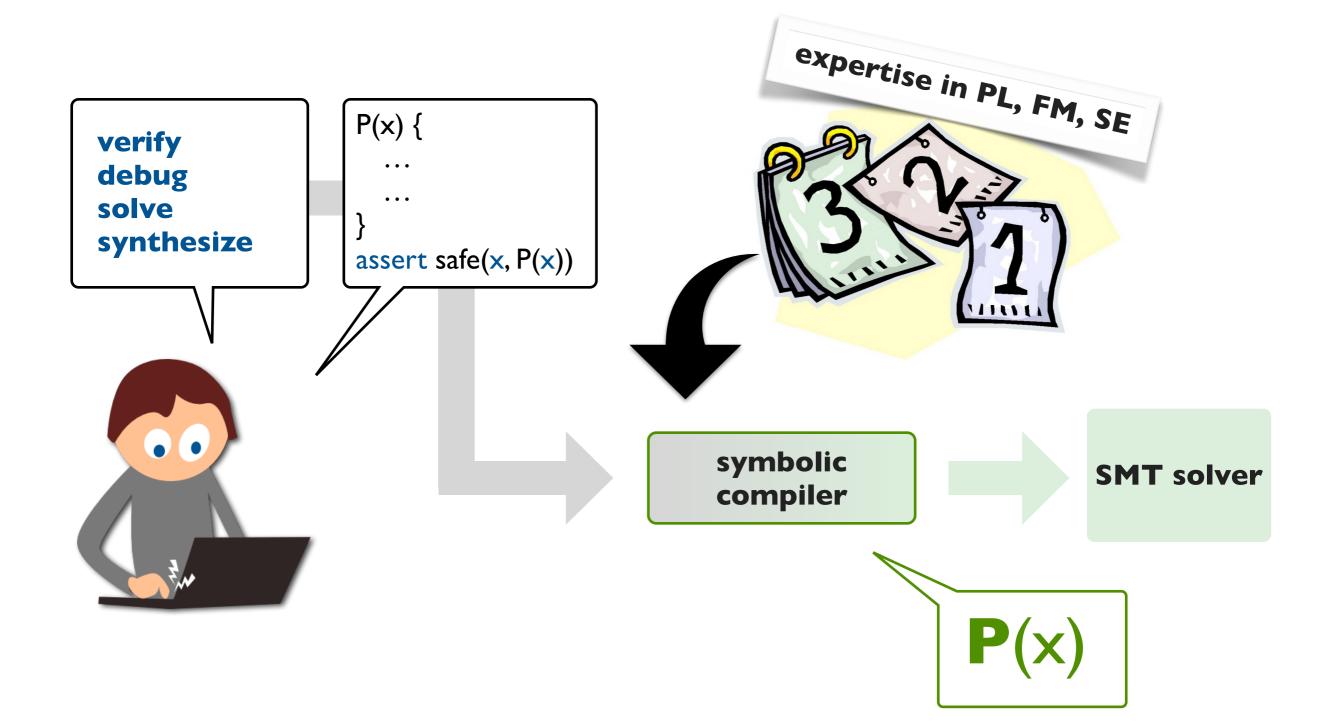


Find an input on which the program fails.Localize bad parts of the program.Find values that repair the failing run.Find code that repairs the program.

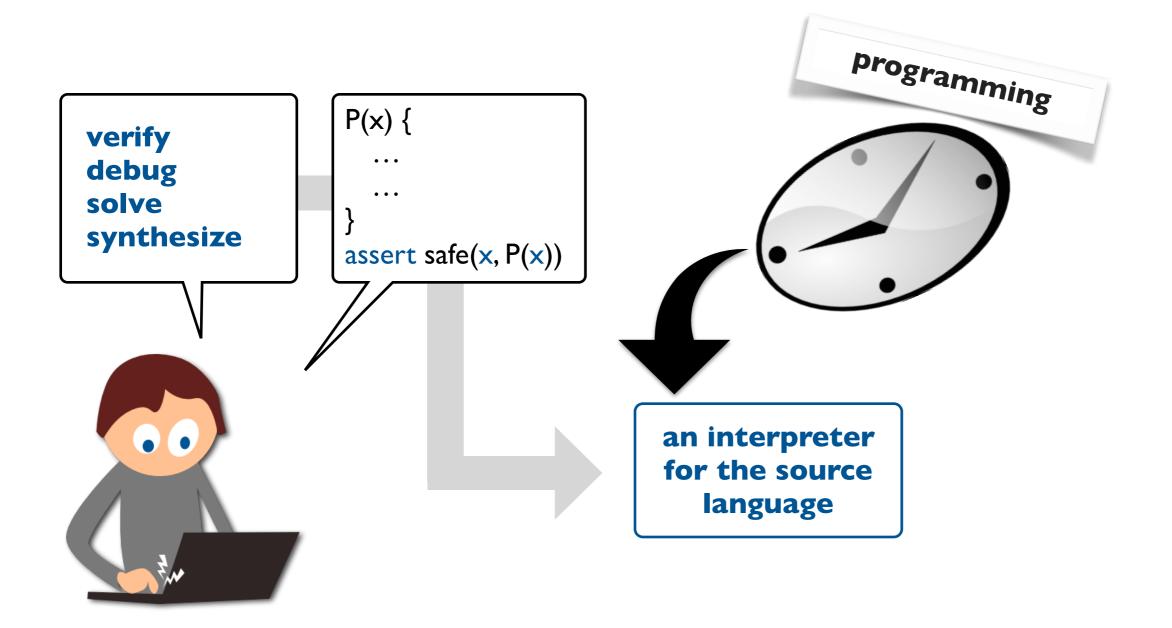




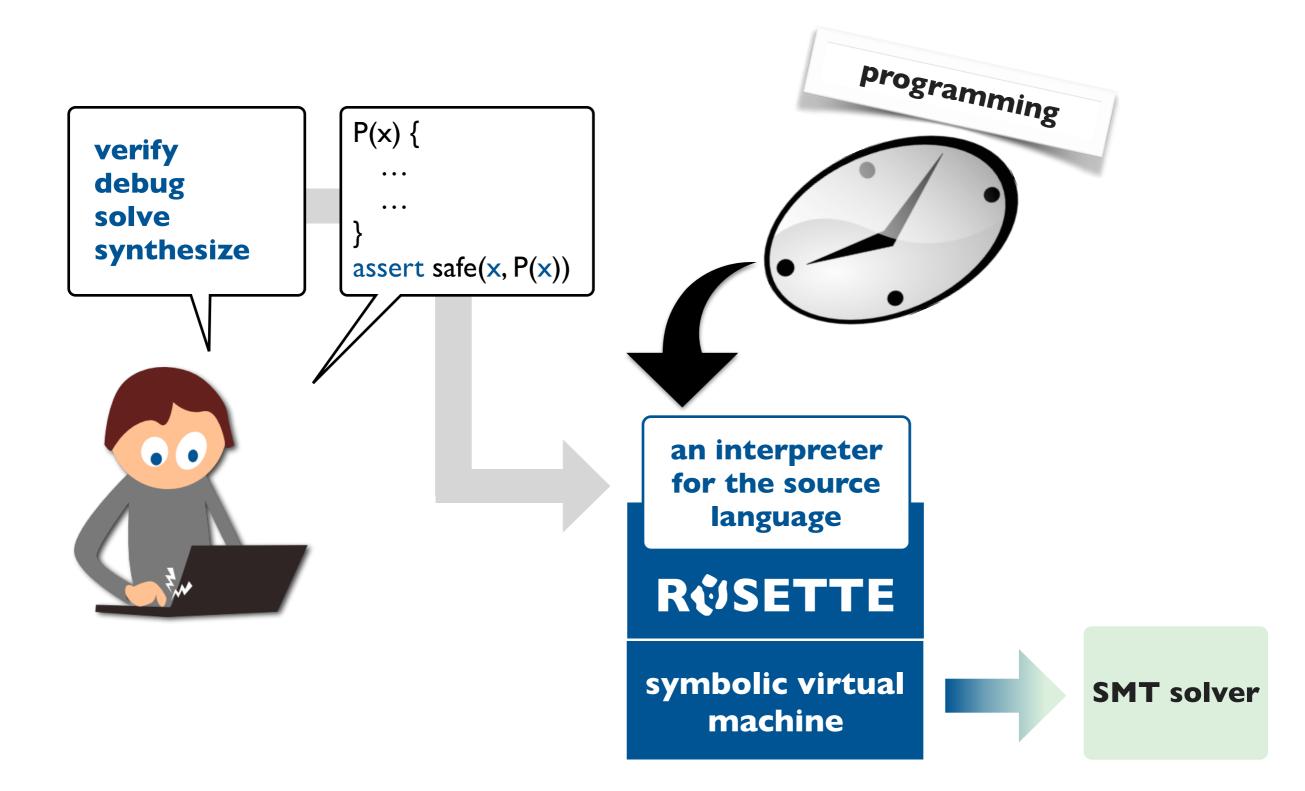




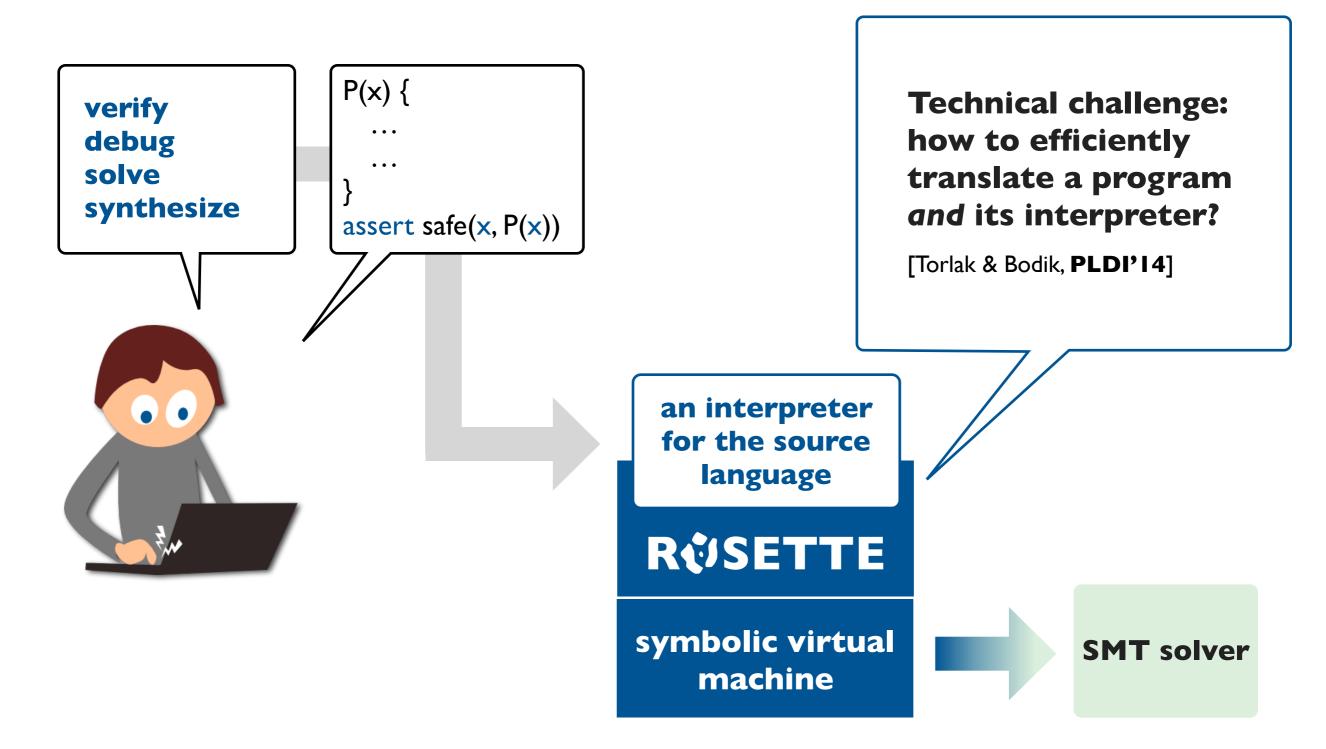
Wanted: an easier way to build tools



Wanted: an easier way to build tools



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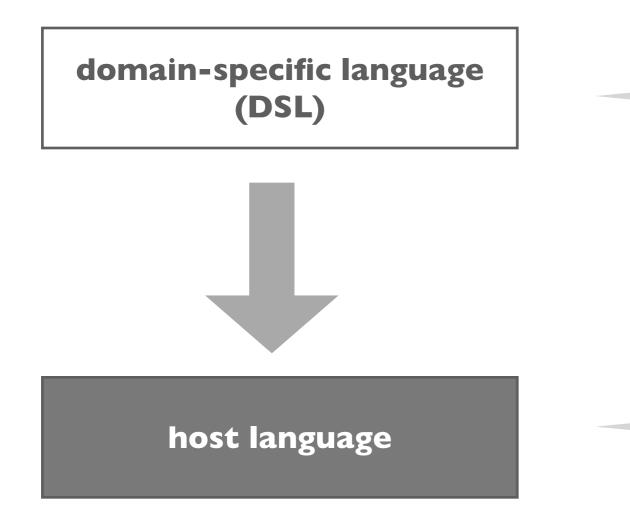
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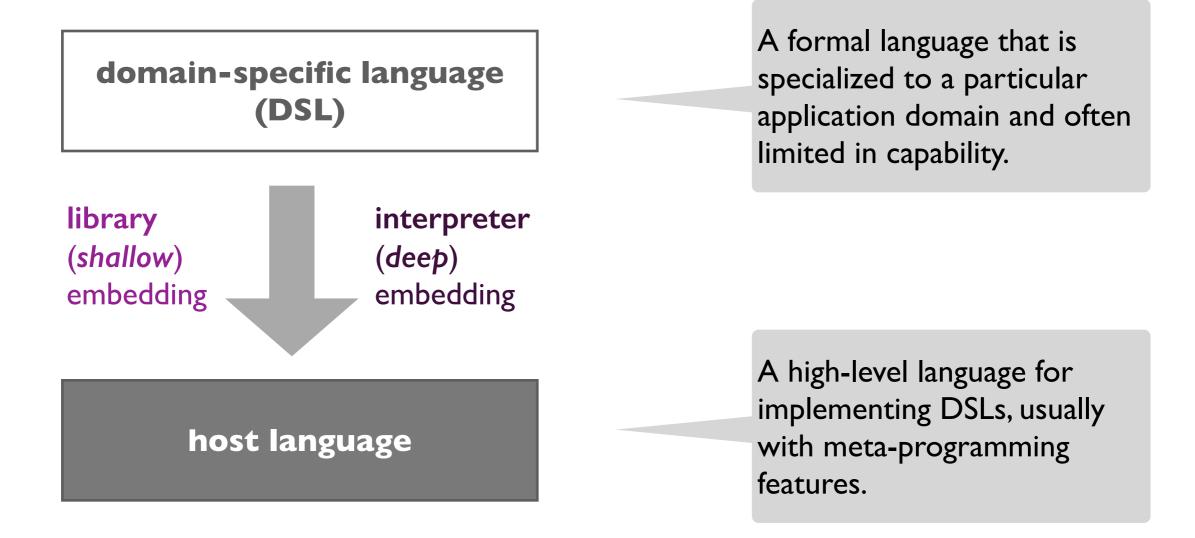
Layers of classic languages: DSLs and hosts



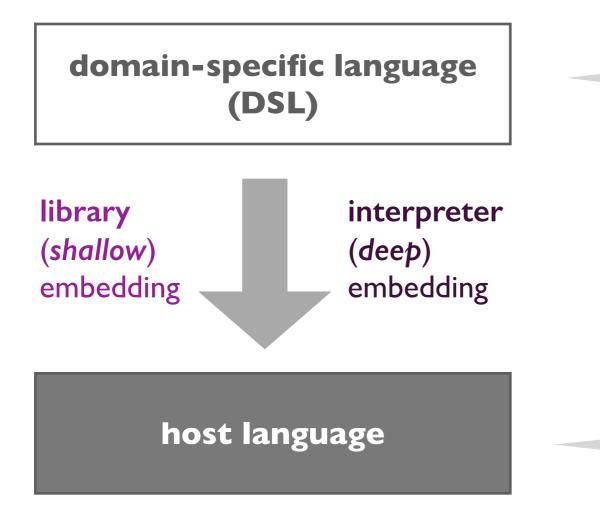
A formal language that is specialized to a particular application domain and often limited in capability.

A high-level language for implementing DSLs, usually with meta-programming features.

Layers of classic languages: DSLs and hosts



Layers of classic languages: many DSLs and hosts



artificial intelligence Church, BLOG

databases SQL, Datalog

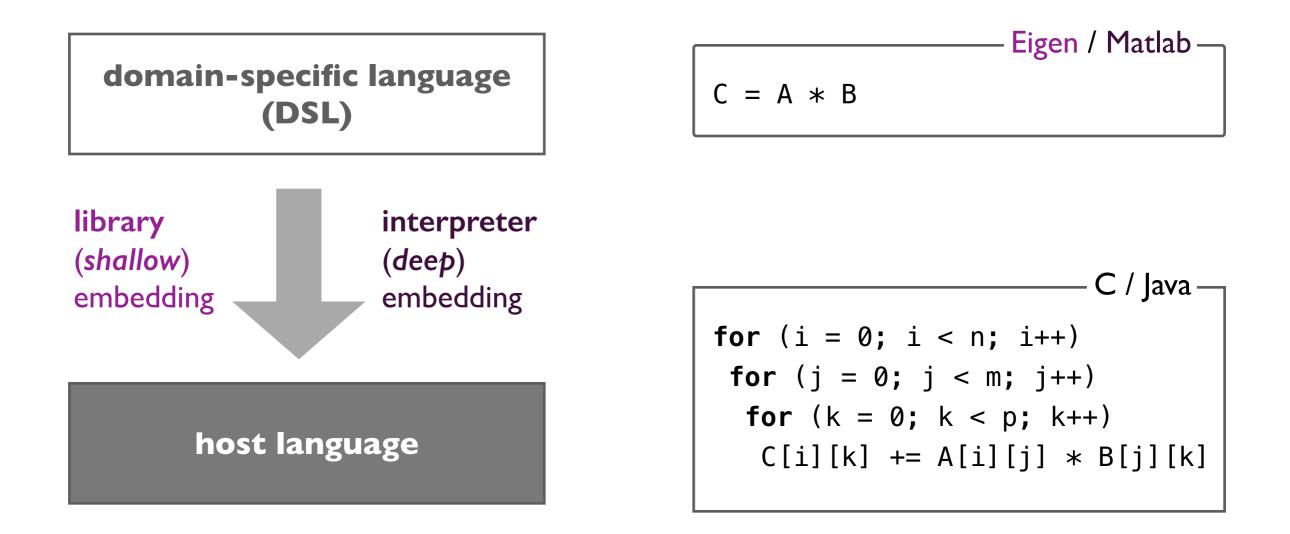
hardware design Bluespec, Chisel, Verilog, VHDL

math and statistics Eigen, Matlab, R

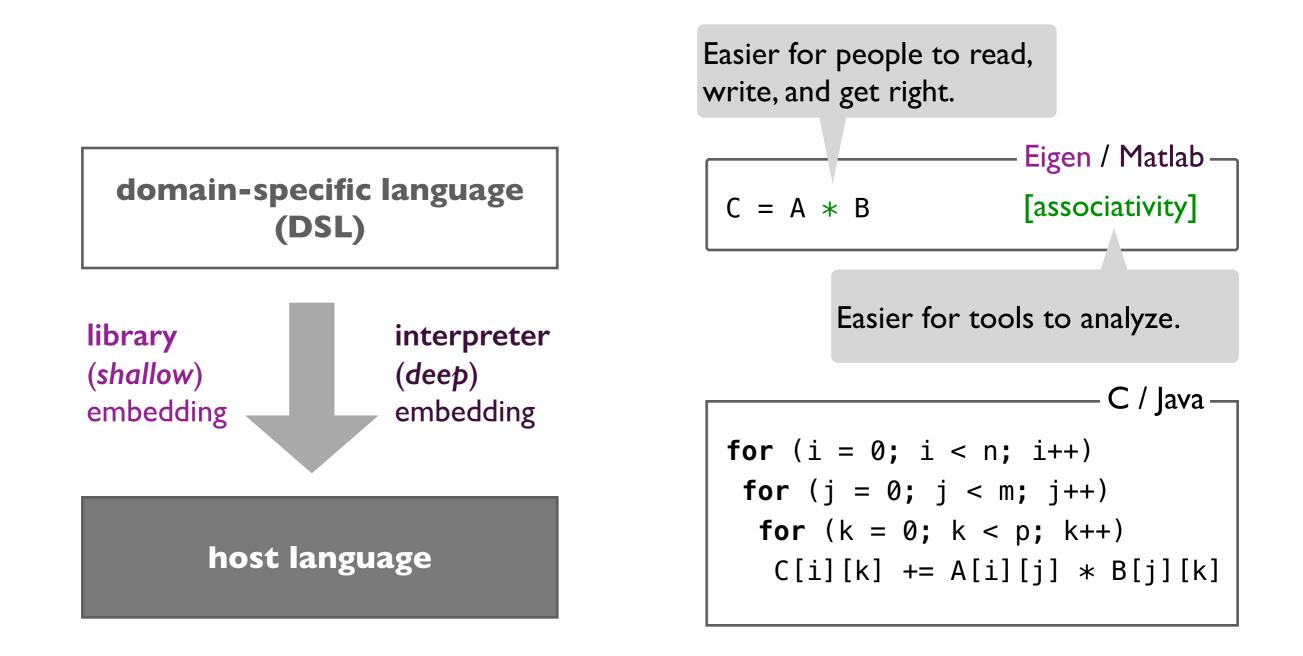
layout and visualization LaTex, dot, dygraphs, D3

Racket, Scala, JavaScript, ...

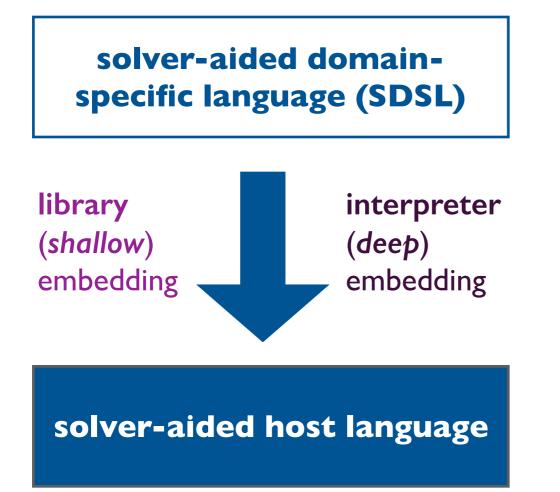
Layers of classic languages: why DSLs?



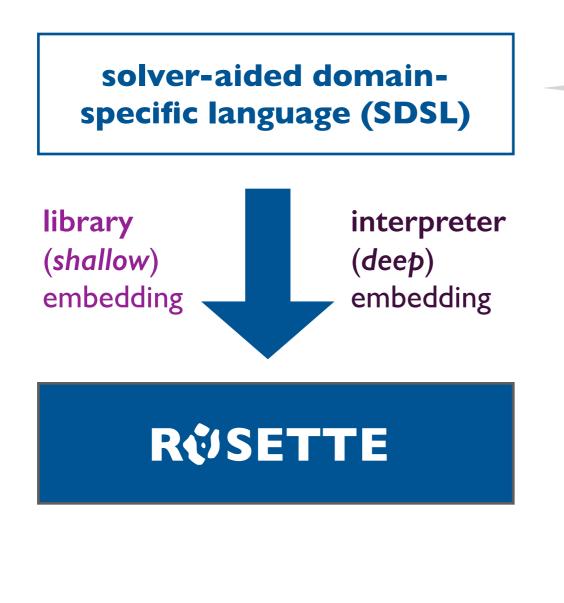
Layers of classic languages: why DSLs?



Layers of solver-aided languages



Layers of solver-aided languages: tools as SDSLs



education and games

Enlearn, RuleSy (VMCAI'18), Nonograms (FDG'17), UCB feedback generator (ITiCSE'17)

synthesis-aided compilation

LinkiTools, Chlorophyll (PLDI'14), GreenThumb (ASPLOS'16)

type system soundness Bonsai (POPI'18)

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computer architecture

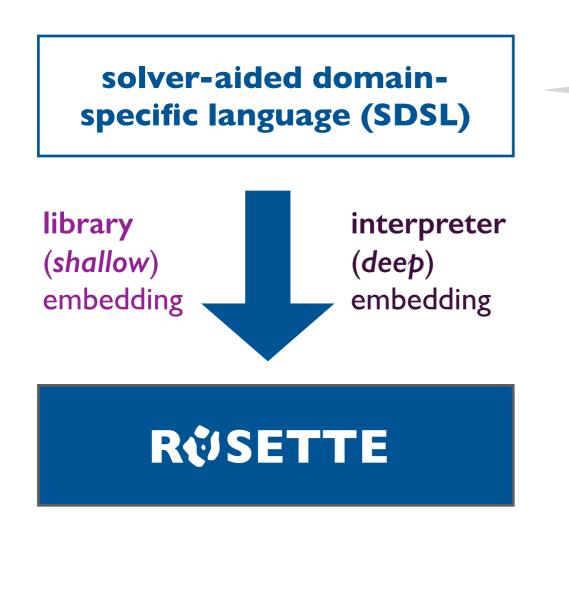
MemSynth (PLDI'17)

databases Cosette (CIDR'17)

radiation therapy control Neutrons (CAV'16)

... and more

Layers of solver-aided languages: tools as SDSLs



education and games Enlearn, RuleSy (VMCAI'18), Nonograms (FDG'17), UCB feedback generator (ITiCSE'17)

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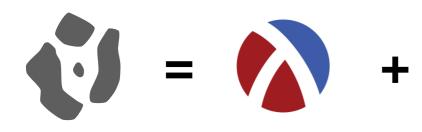
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... and more

The anatomy of a solver-aided host language



<pre>(define-symbolic id type) (define-symbolic* id type)</pre>	symbolic values
(assert expr)	assertions
<pre>(verify expr) (debug [type+] expr)</pre>	
(solve expr)	queries
(synthesize	
#:forall expr	
<pre>#:guarantee expr)</pre>	

```
def bvmax(r0, r1) :
    r2 = bvsge(r0, r1)
    r3 = bvneg(r2)
    r4 = bvxor(r0, r2)
    r5 = bvand(r3, r4)
    r6 = bvxor(r1, r5)
    return r6
```

BV: A tiny assembly-like language for writing fast, low-level library functions.

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def bvmax(r0, r1) :
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We want to **test**, **verify**, **debug**, and **synthesize** programs in the BV SDSL. **BV**: A tiny assembly-like language for writing fast, low-level library functions.

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We want to **test**, **verify**, **debug**, and **synthesize** programs in the BV SDSL.

BV: A tiny assembly-like language for writing fast, low-level library functions.

١.	interpreter	[10 LOC]
2.	verifier	[free]
3.	debugger	[free]
4.	synthesizer	[free]

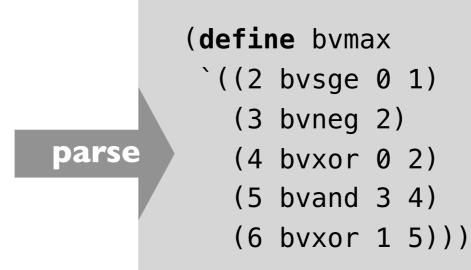
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```
> bvmax(-2, -1)
```

R¢SETTE

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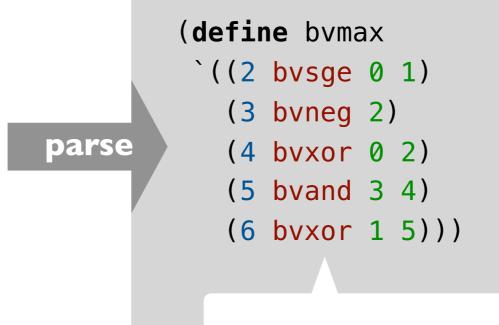
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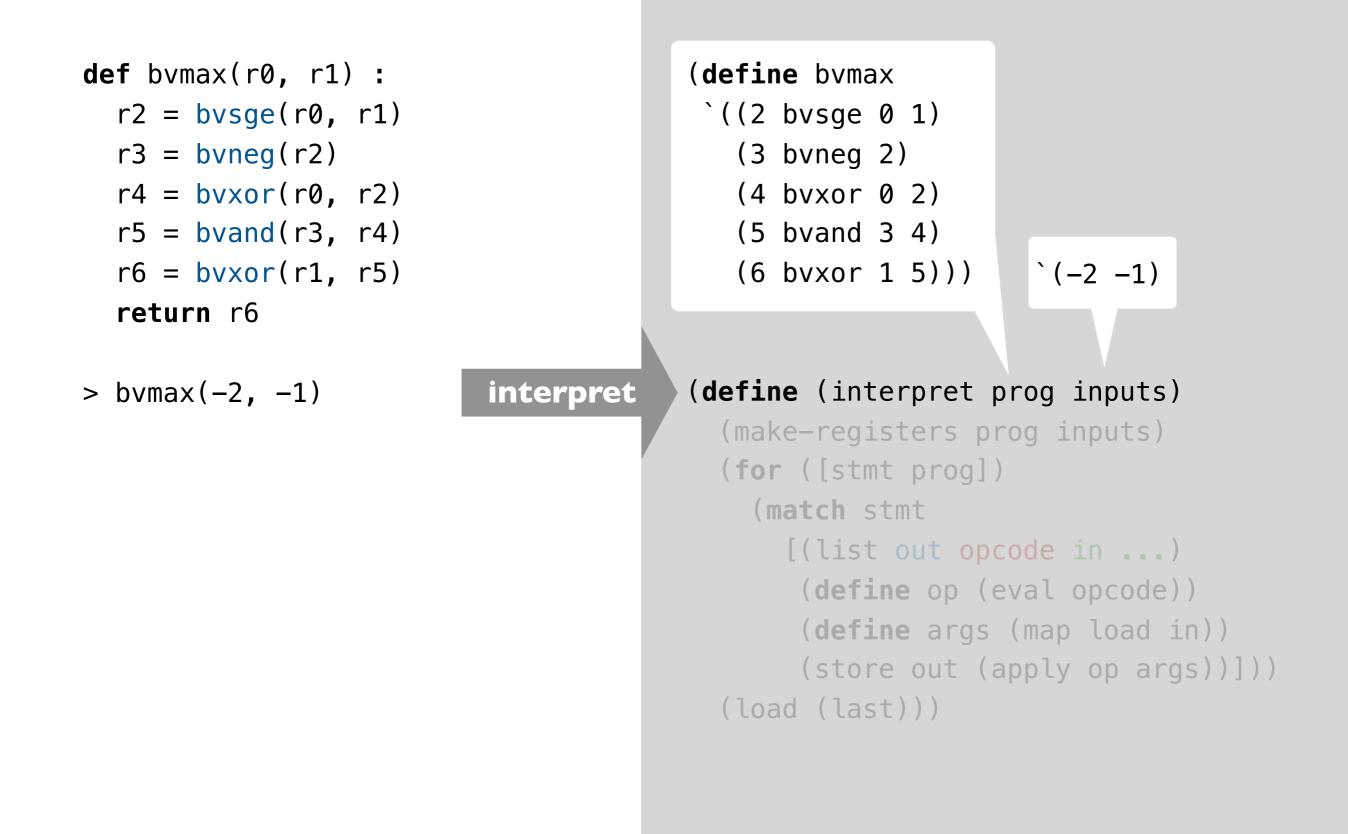
R¢SETTE

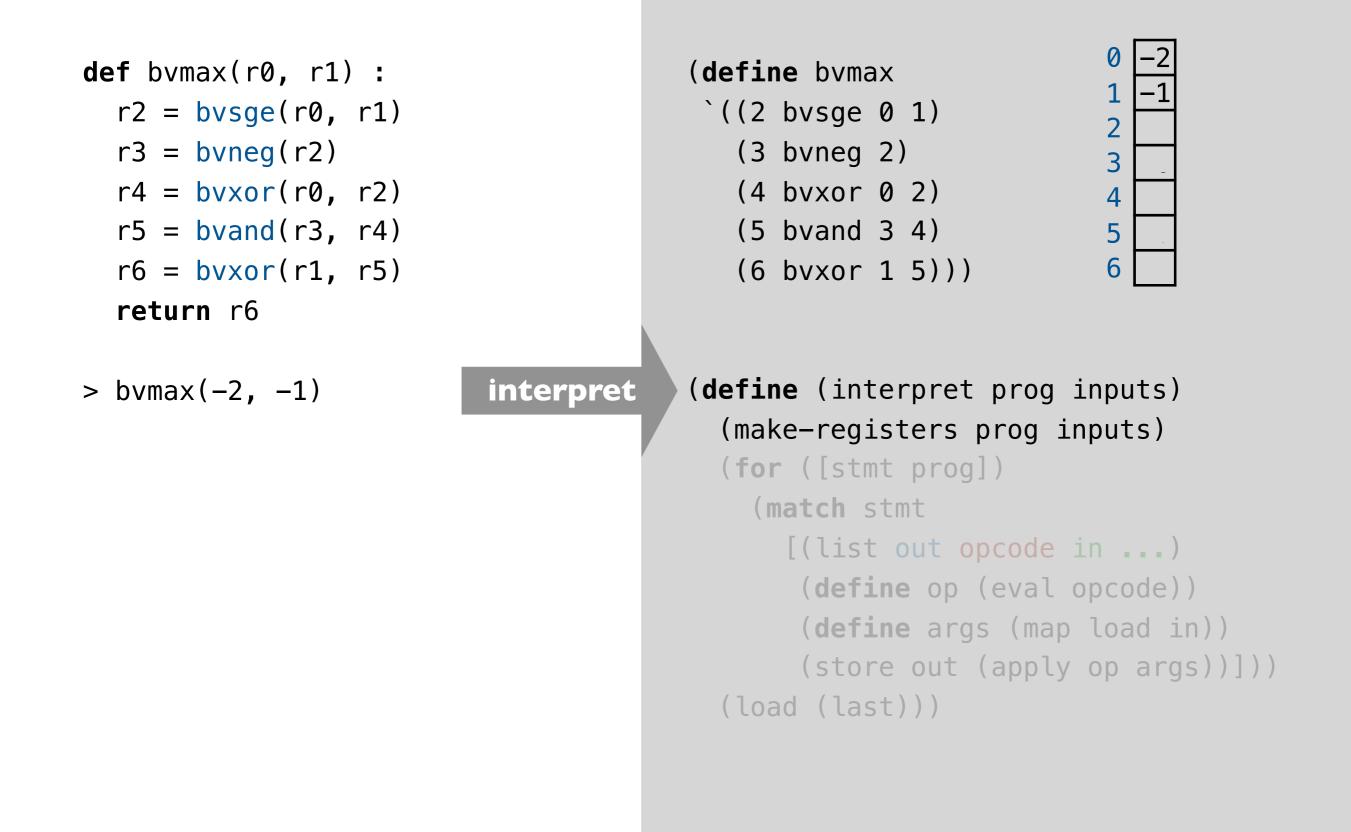
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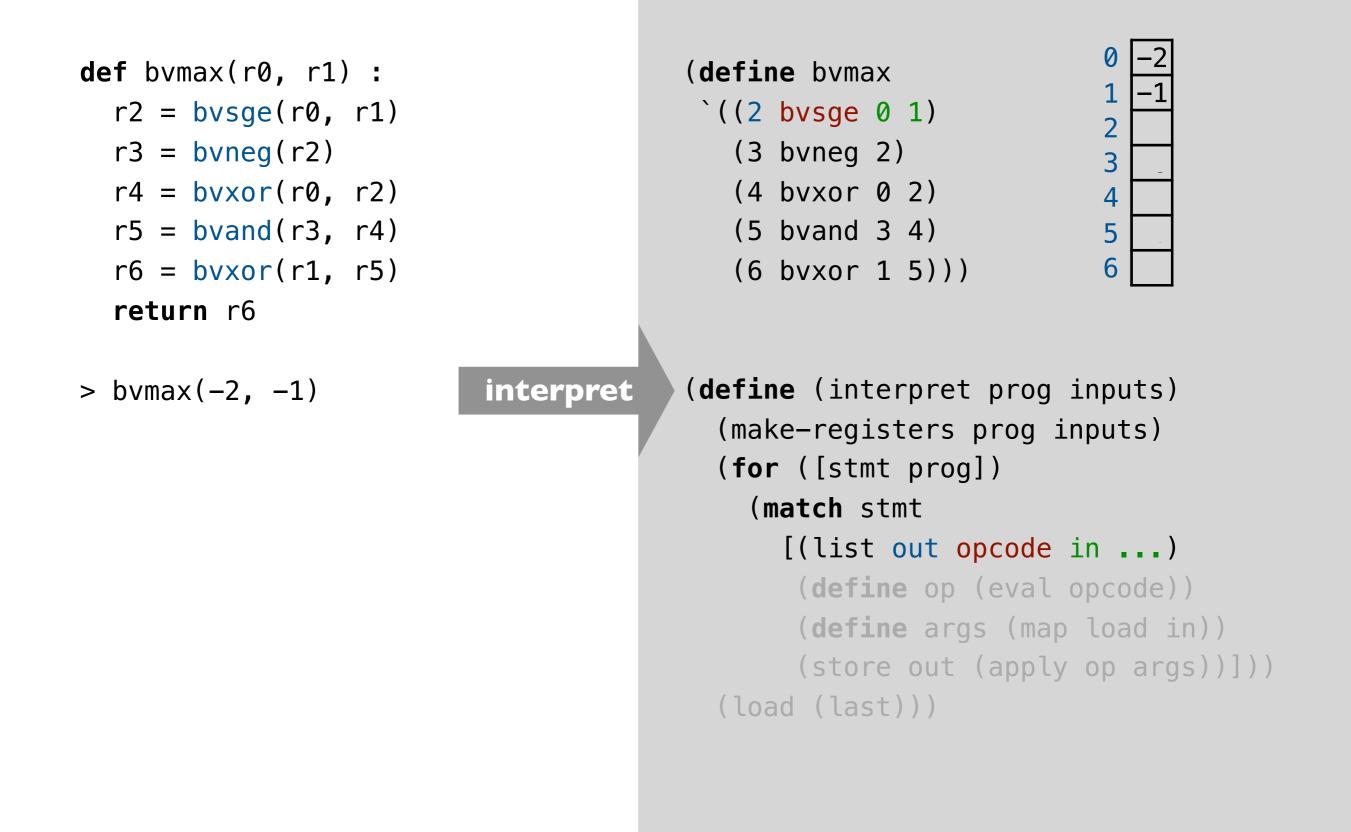
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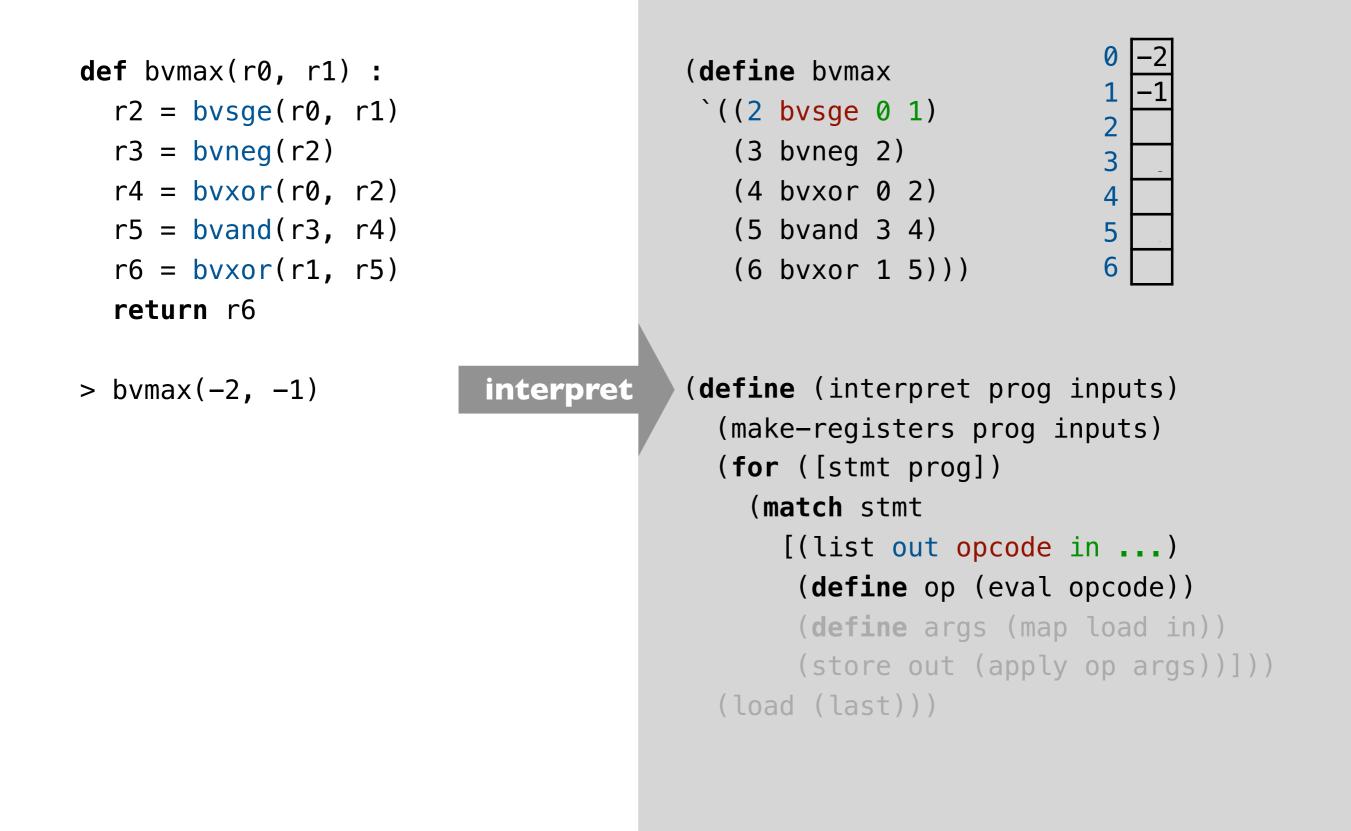


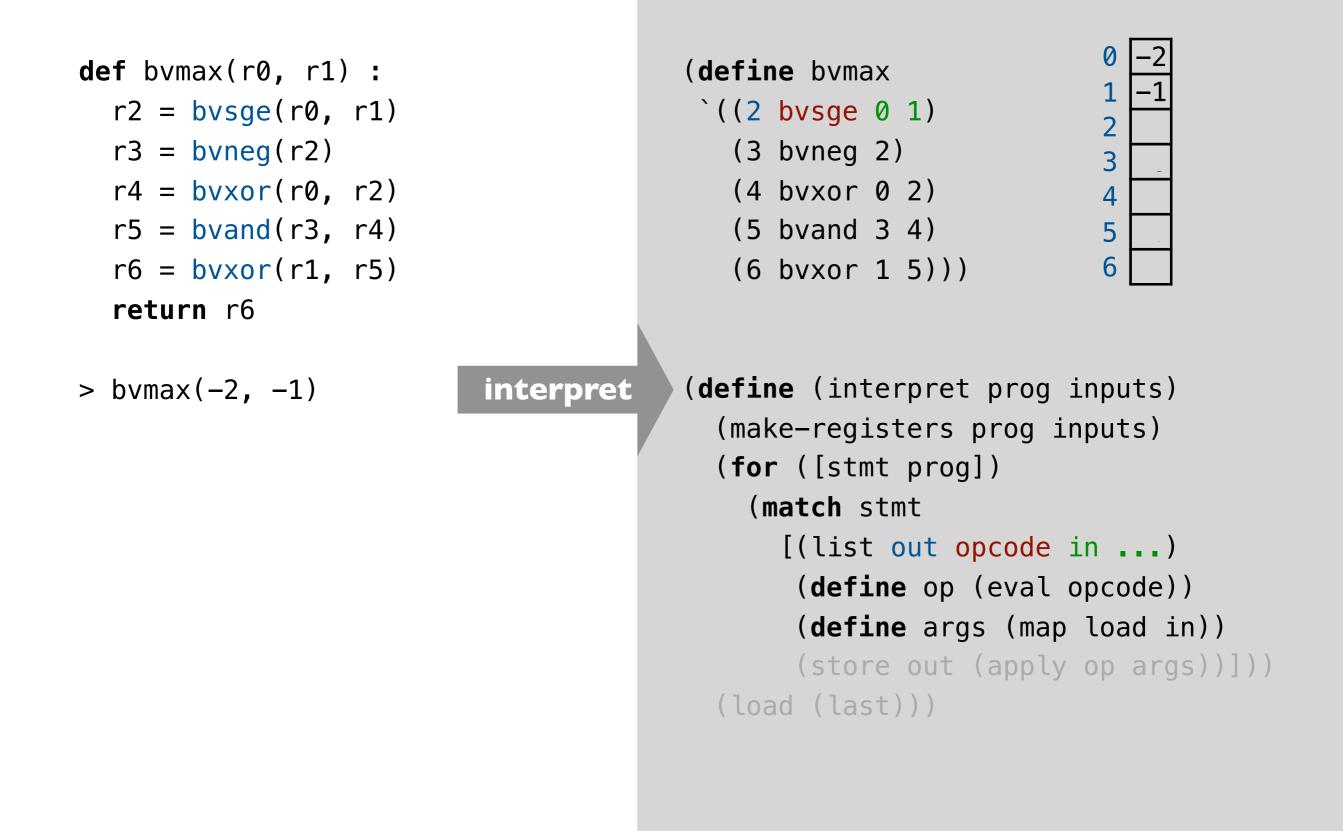
(out opcode in ...)

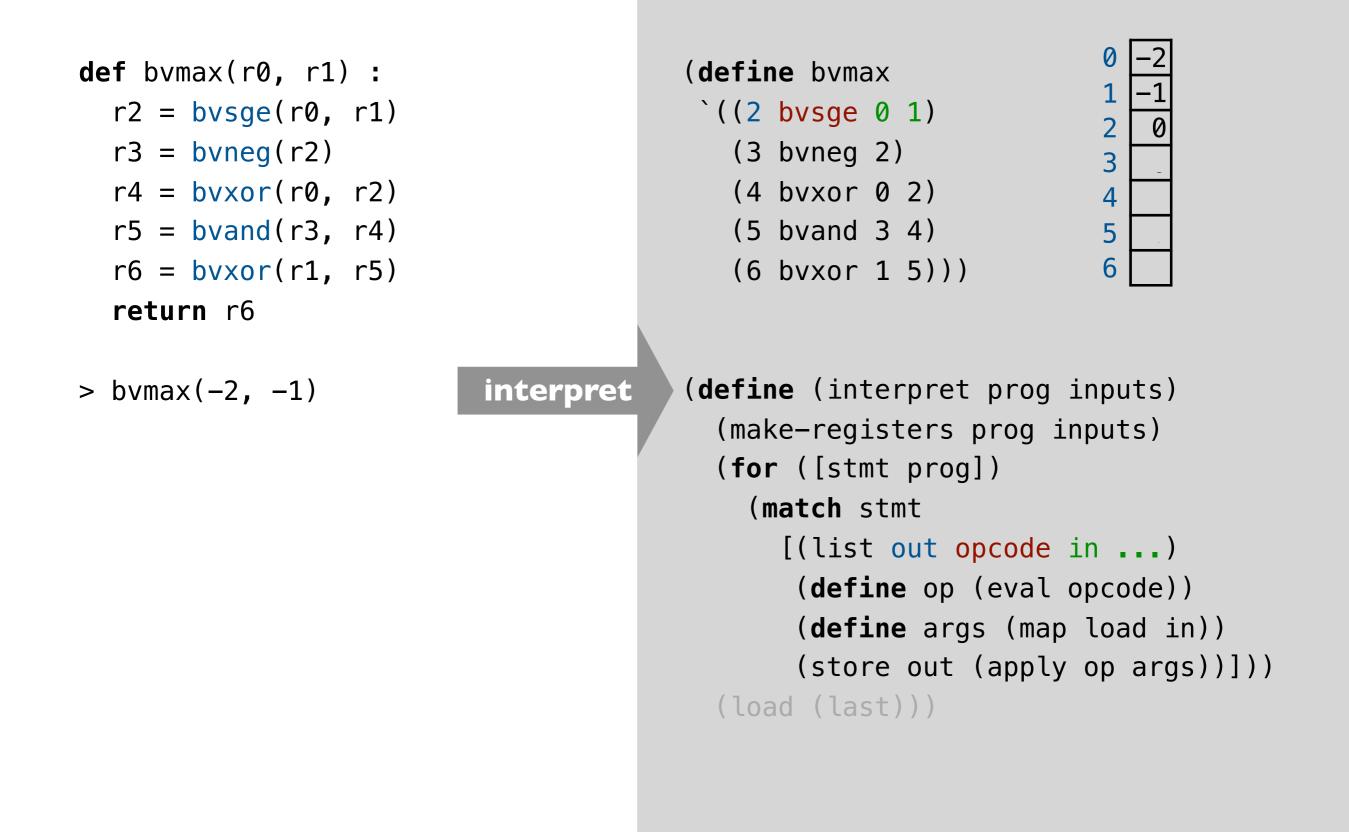












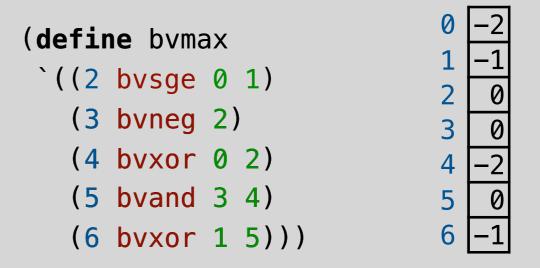
R

<pre>def bvmax(r0, r1) : r2 = bvsge(r0, r1) r3 = bvneg(r2) r4 = bvxor(r0, r2) r5 = bvand(r3, r4) r6 = bvxor(r1, r5)</pre>	<pre>(define bvmax 0 -2 `((2 bvsge 0 1) 2 0 (3 bvneg 2) 3 0 (4 bvxor 0 2) 4 -2 (5 bvand 3 4) 5 0 (6 bvxor 1 5))) 6 -1</pre>
return r6	
> bvmax(-2, -1) interpret	<pre>(define (interpret prog inputs) (make-registers prog inputs) (for ([stmt prog]) (match stmt [(list out opcode in) (define op (eval opcode)) (define args (map load in)) (store out (apply op args))])) (load (last)))</pre>

R**i**SETTE

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```

interpret



```
(define (interpret prog inputs)
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  (for ([stmt prog])
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```

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    return r6
```

```
> bvmax(-2, -1)
-1
```

(**define** bvmax

- `((2 bvsge 0 1)
 - (3 bvneg 2)
 - (4 bvxor 0 2)
 - (5 bvand 3 4)
 - (6 bvxor 1 5)))

pattern matching

- dynamic evaluation
- first-class & higherorder procedures
- side effects

```
(define (interpret prog inputs)
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> verify(bvmax, max)

query

R**i**SETTE

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(0, -2)
```



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```
> verify(bvmax, max)
(0, -2)
```

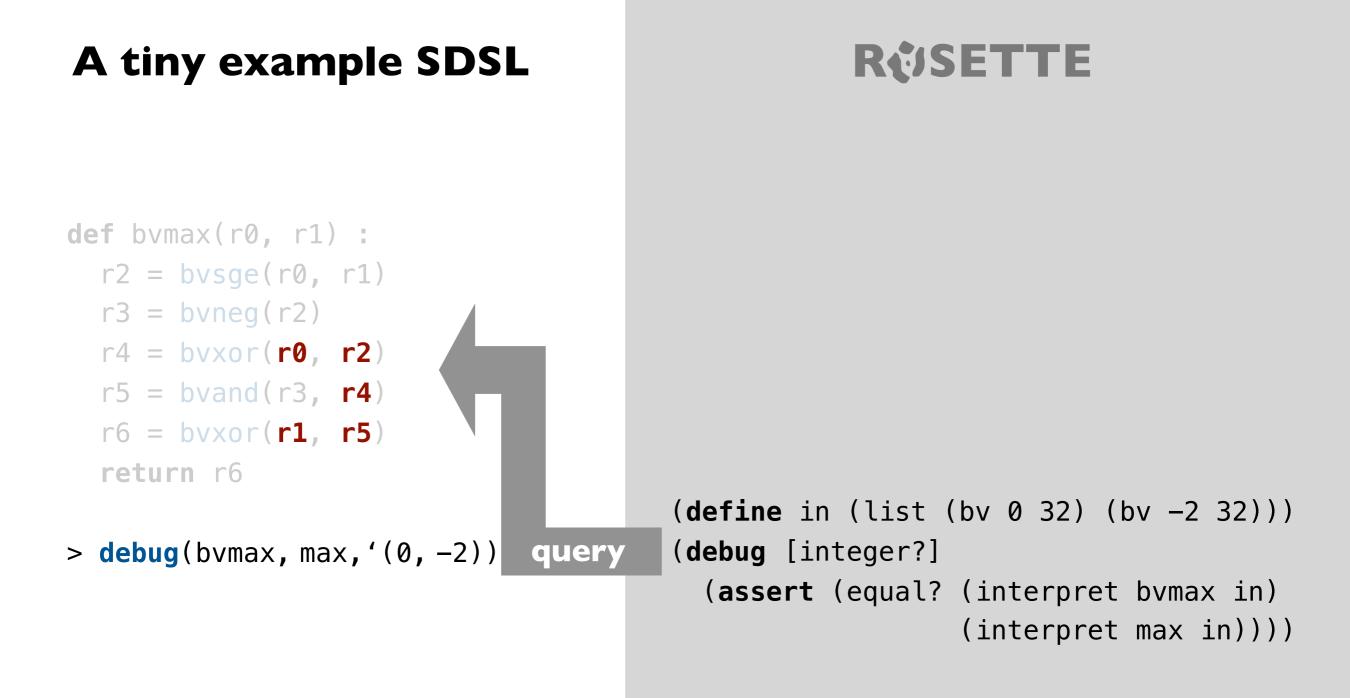
```
> bvmax(0, -2)
-1
```



RiSETTE

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    r5 = bvand(r3, r4)
    r6 = bvxor(r1, r5)
    return r6
> debug(bvmax, max, '(0, -2)) query
    (define in (list (bv 0 32) (bv -2 32)))
    (debug [integer?]
        (assert (equal? (interpret bvmax in)
```

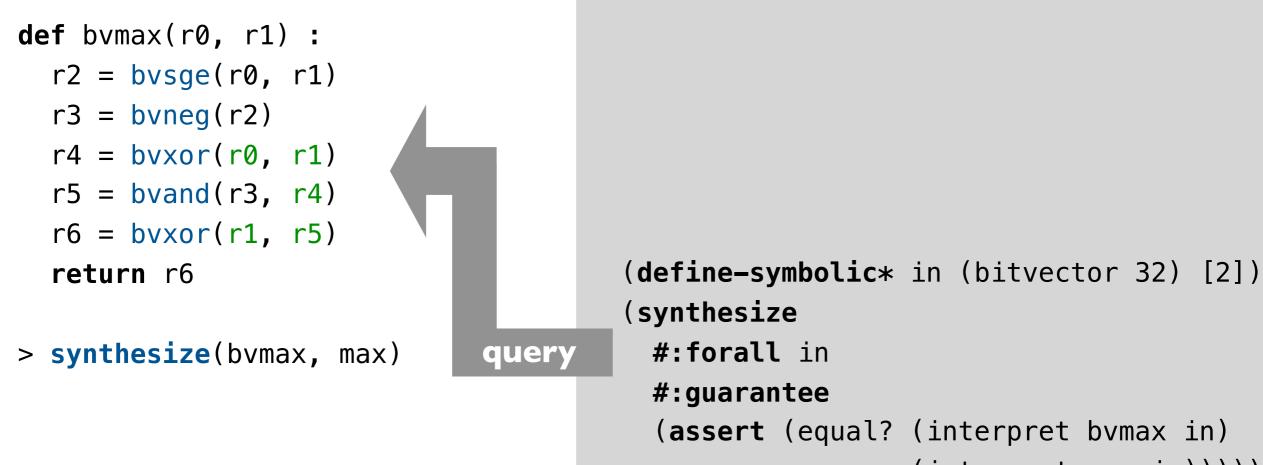
(interpret max in))))



RiSETTE

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RiSETTE



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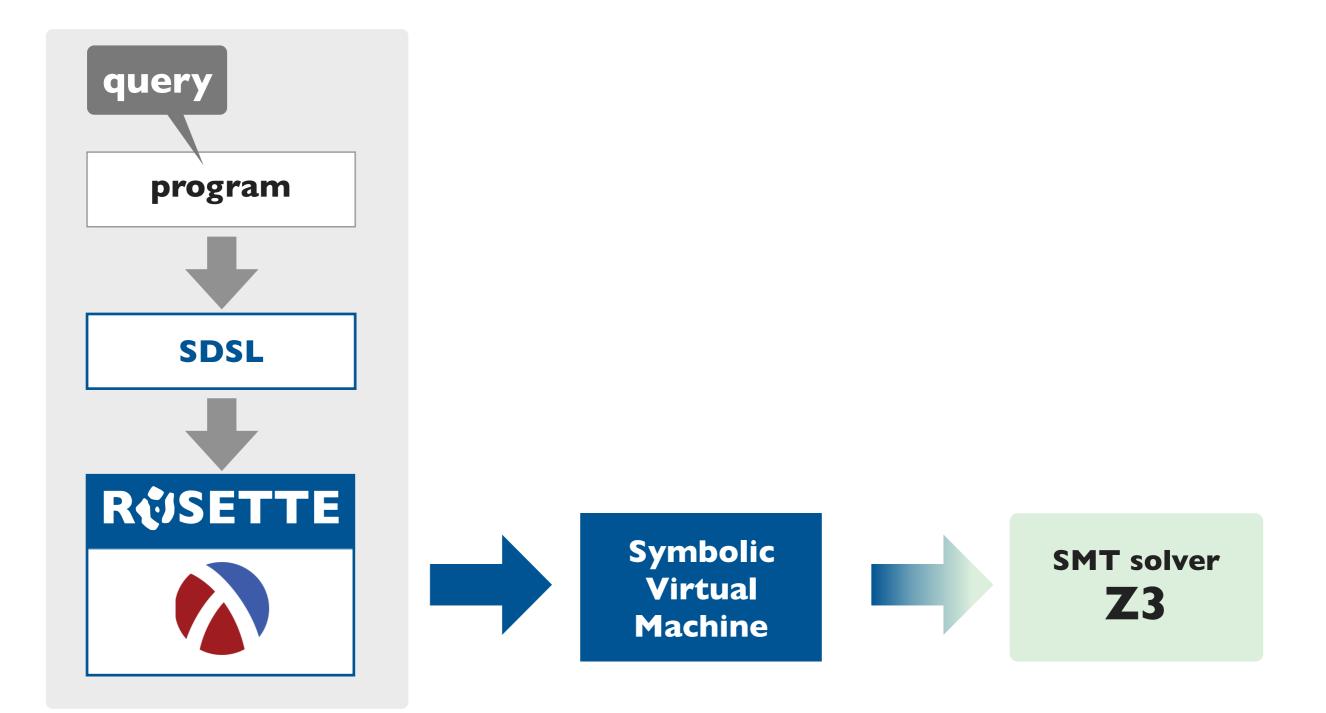
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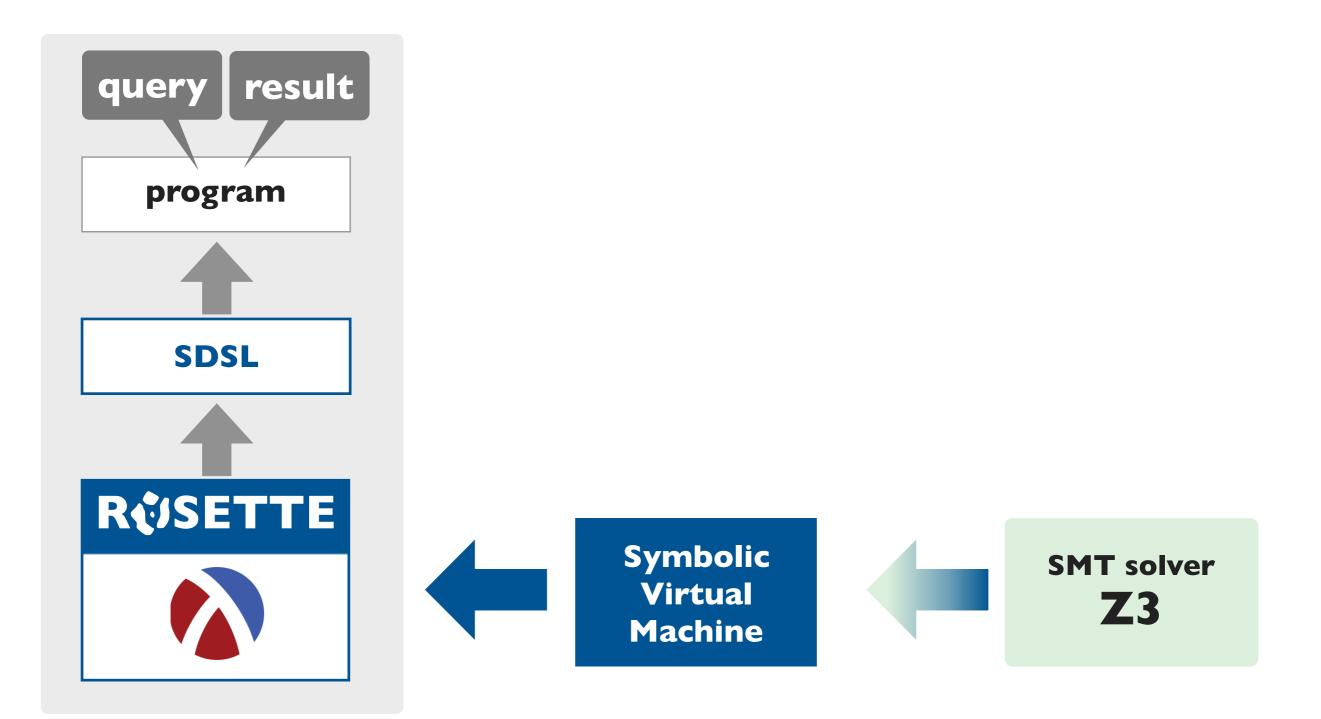
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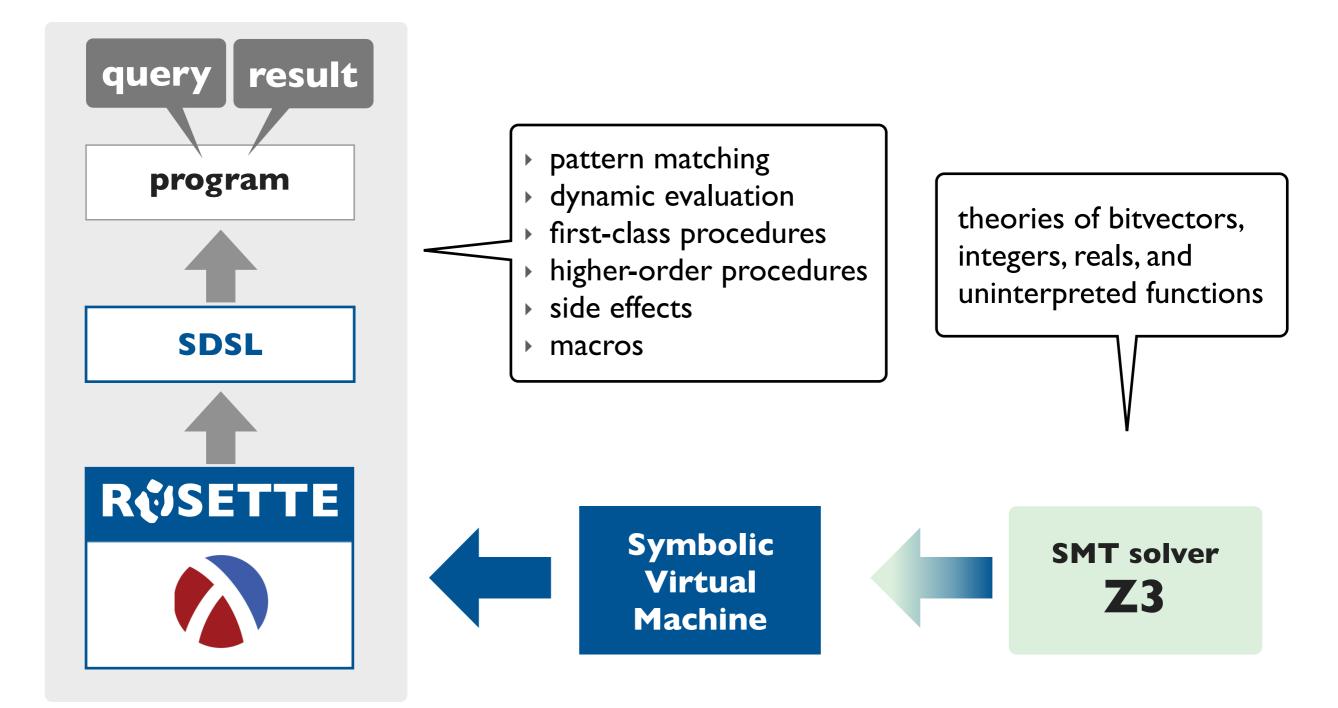
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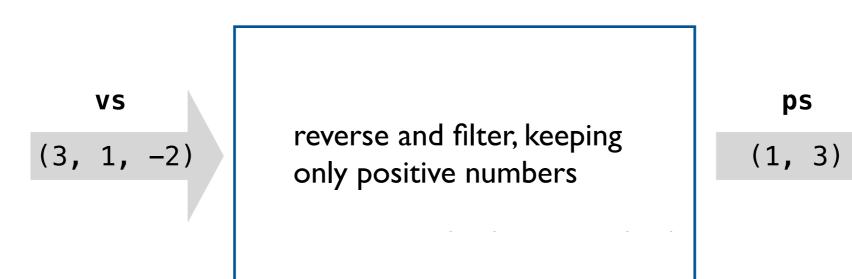


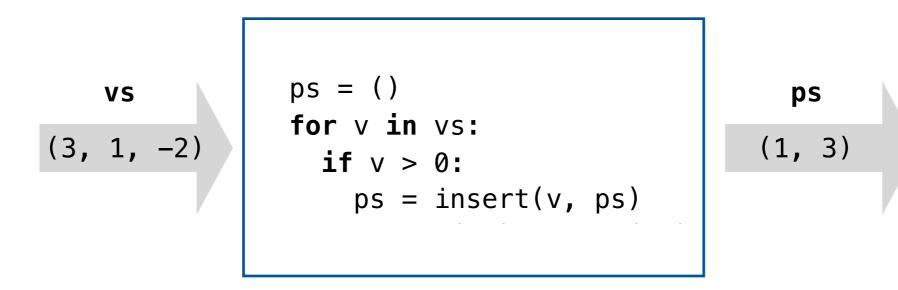
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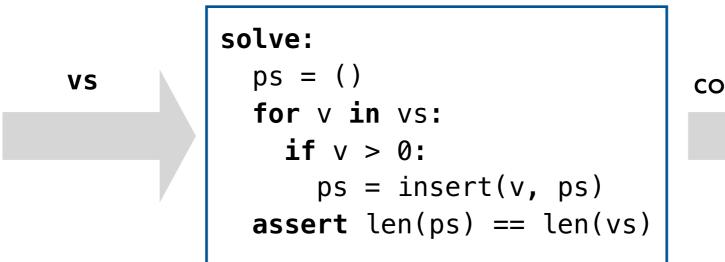


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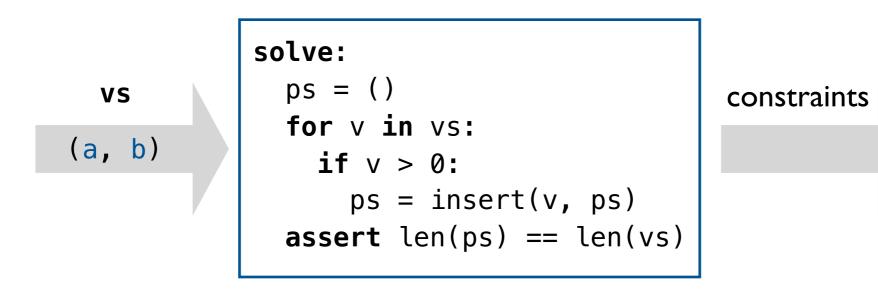


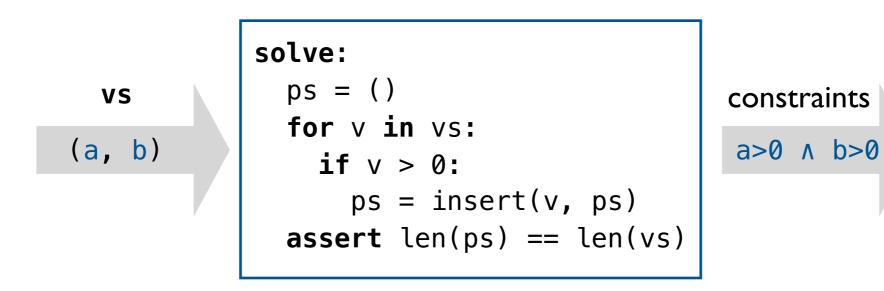


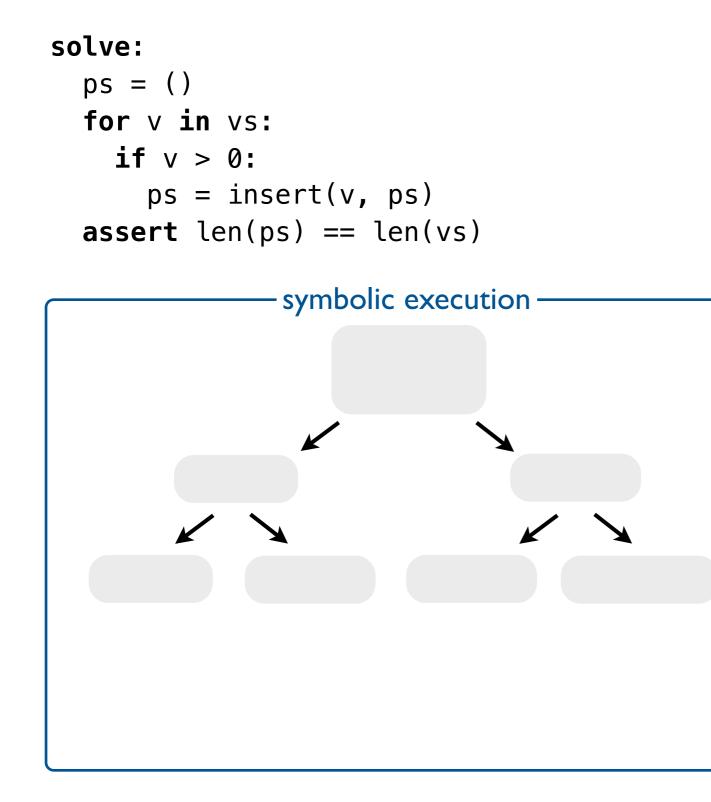


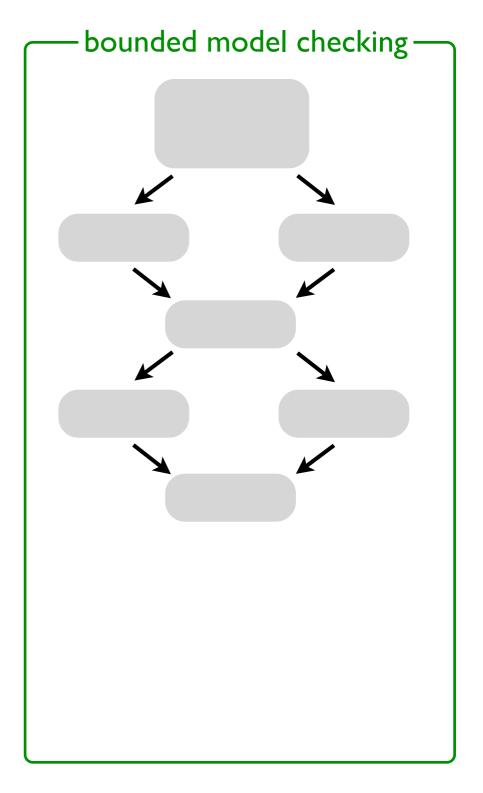


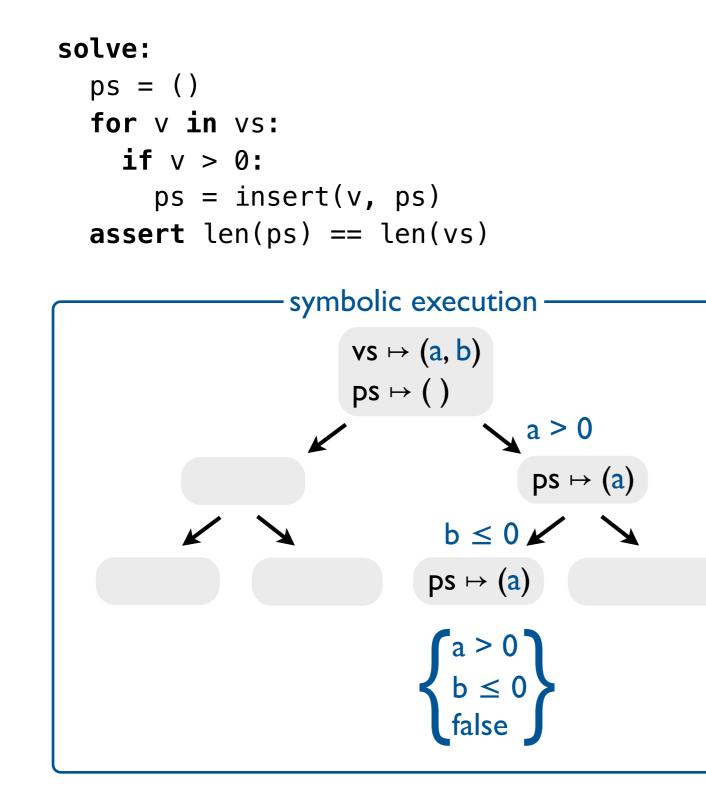
constraints

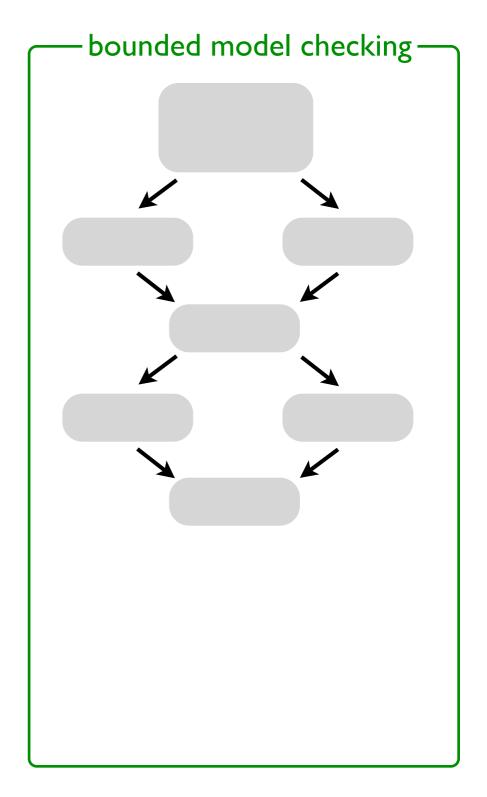




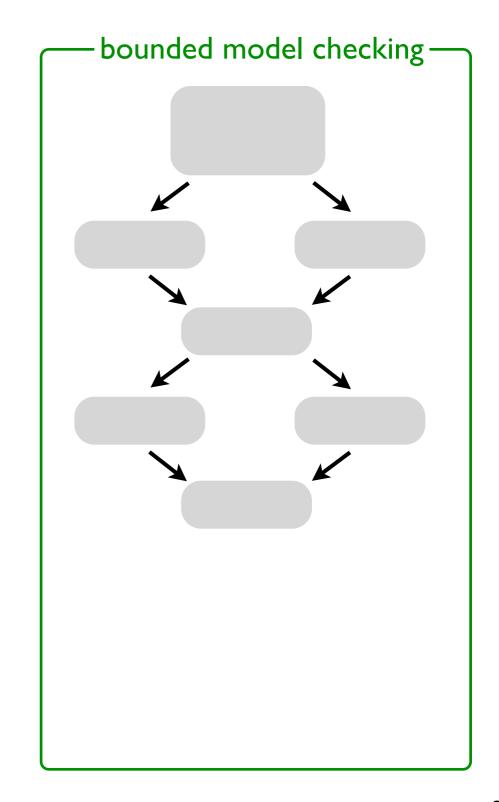




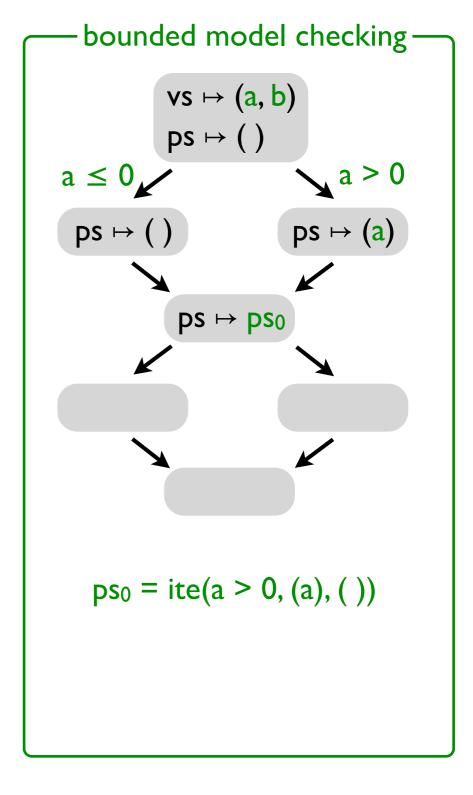




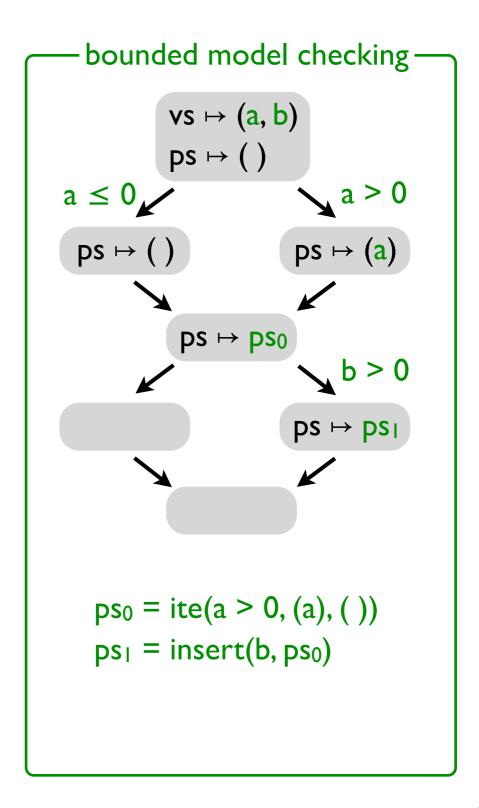
solve: ps = ()for v in vs: if v > 0: ps = insert(v, ps) assert len(ps) == len(vs) symbolic execution $vs \mapsto (a, b)$ $ps \mapsto ()$ $a \le 0 \qquad a \ge 0$ $ps \mapsto ()$ $ps \mapsto (a)$ $b \le 0 \swarrow b > 0$ $b \le 0 \swarrow b > 0$ $ps \mapsto ()$ $ps \mapsto (b)$ $ps \mapsto (a)$ $ps \mapsto (b, a)$ $\begin{cases} a \le 0 \\ b \le 0 \\ false \end{cases} \lor \begin{cases} a \le 0 \\ b > 0 \\ false \end{cases} \lor \begin{cases} a > 0 \\ b \le 0 \\ false \end{cases} \lor \begin{cases} a > 0 \\ b \le 0 \\ false \end{cases} \lor \begin{cases} a > 0 \\ b \ge 0 \\ true \end{cases}$



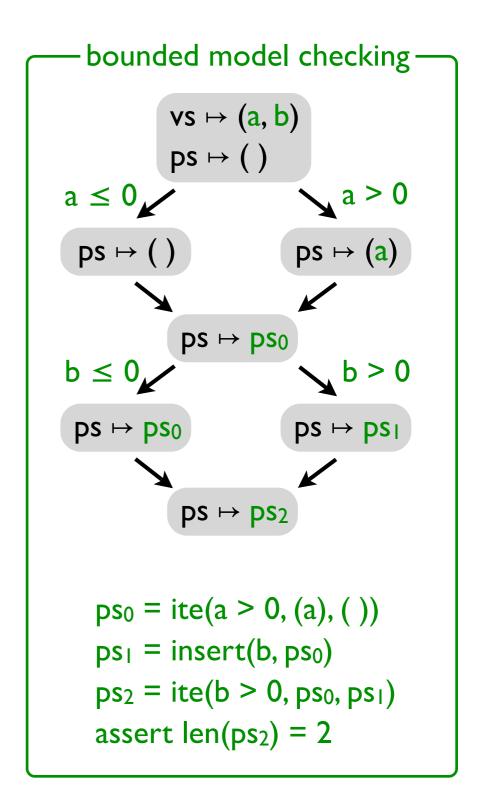
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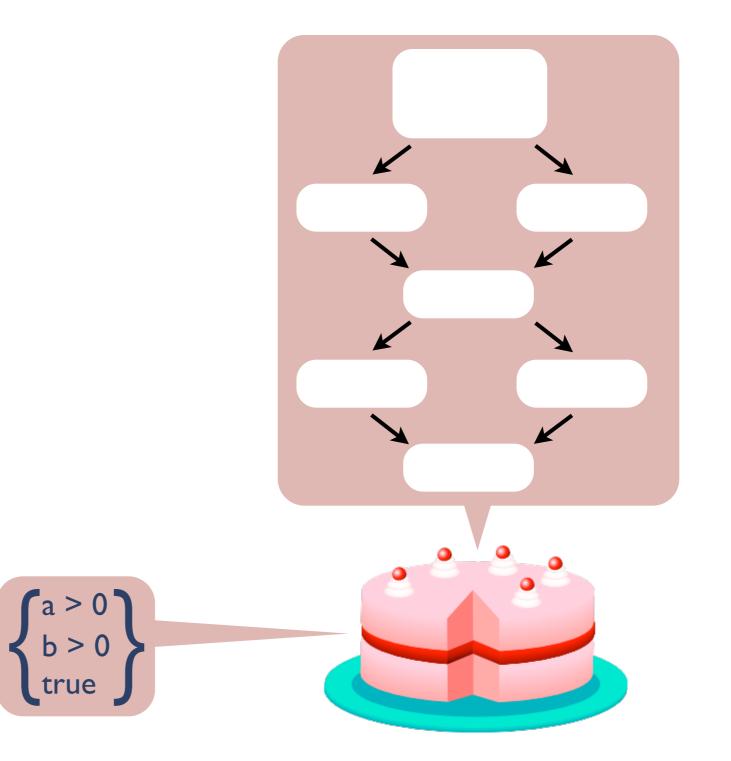
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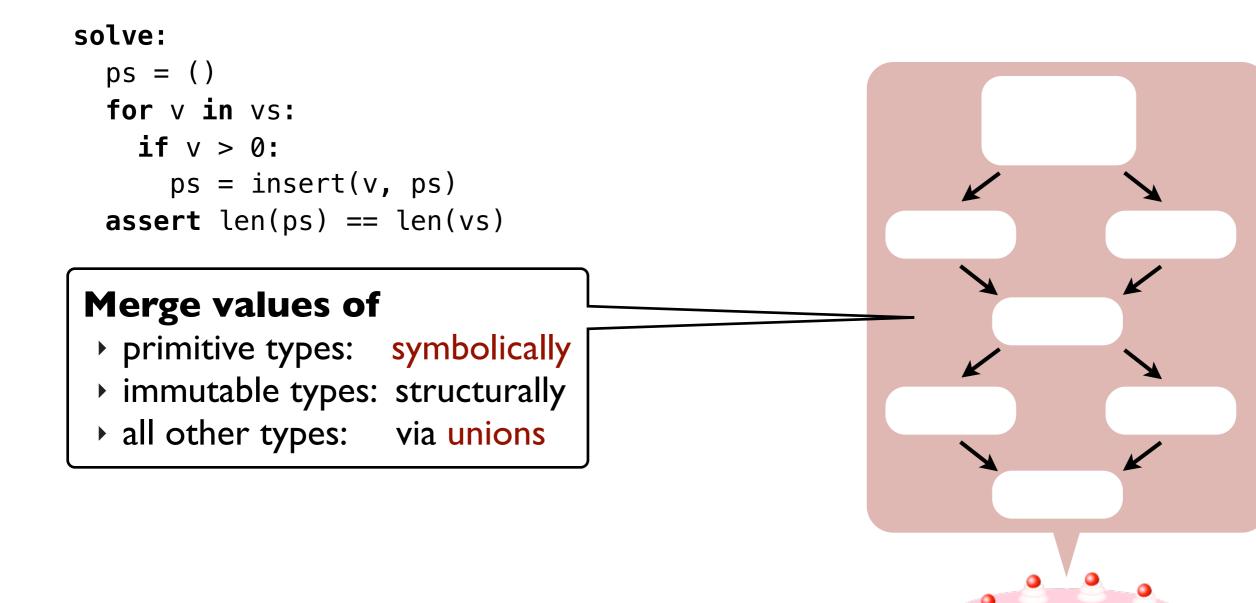


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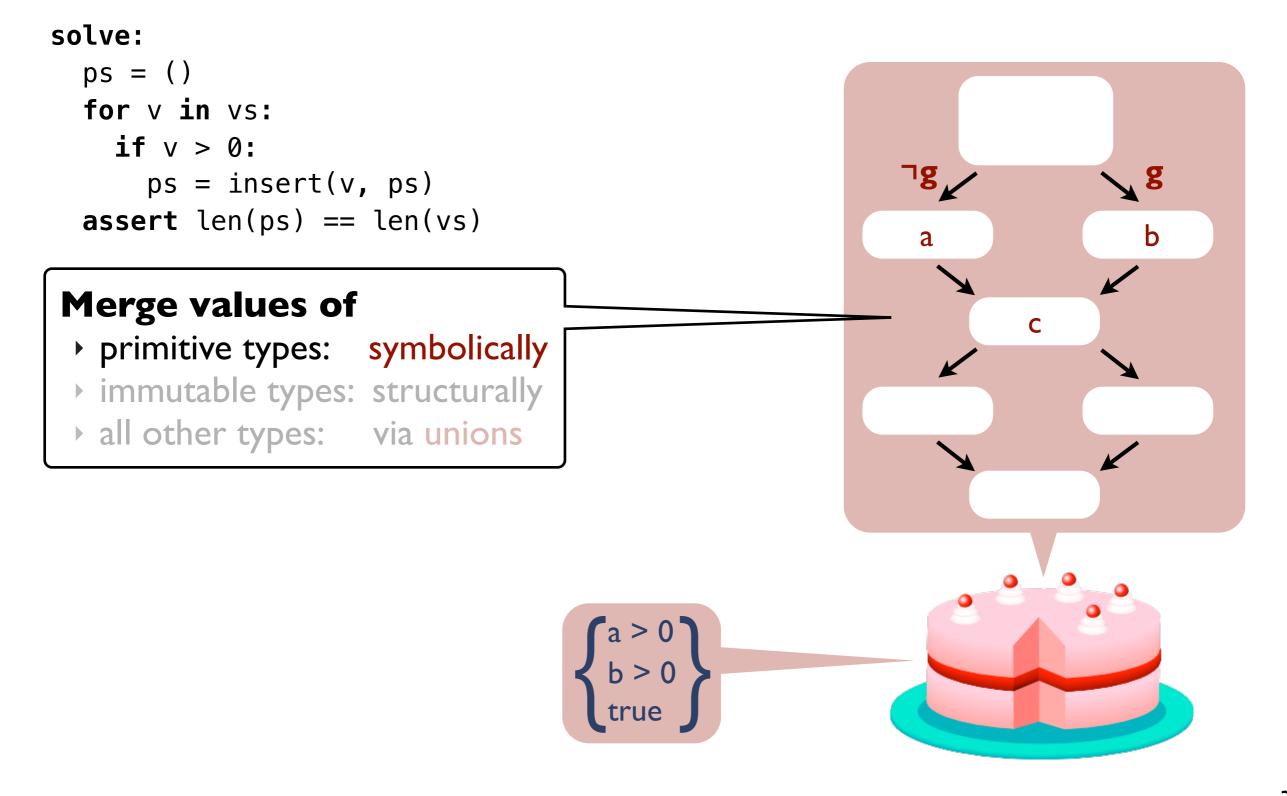


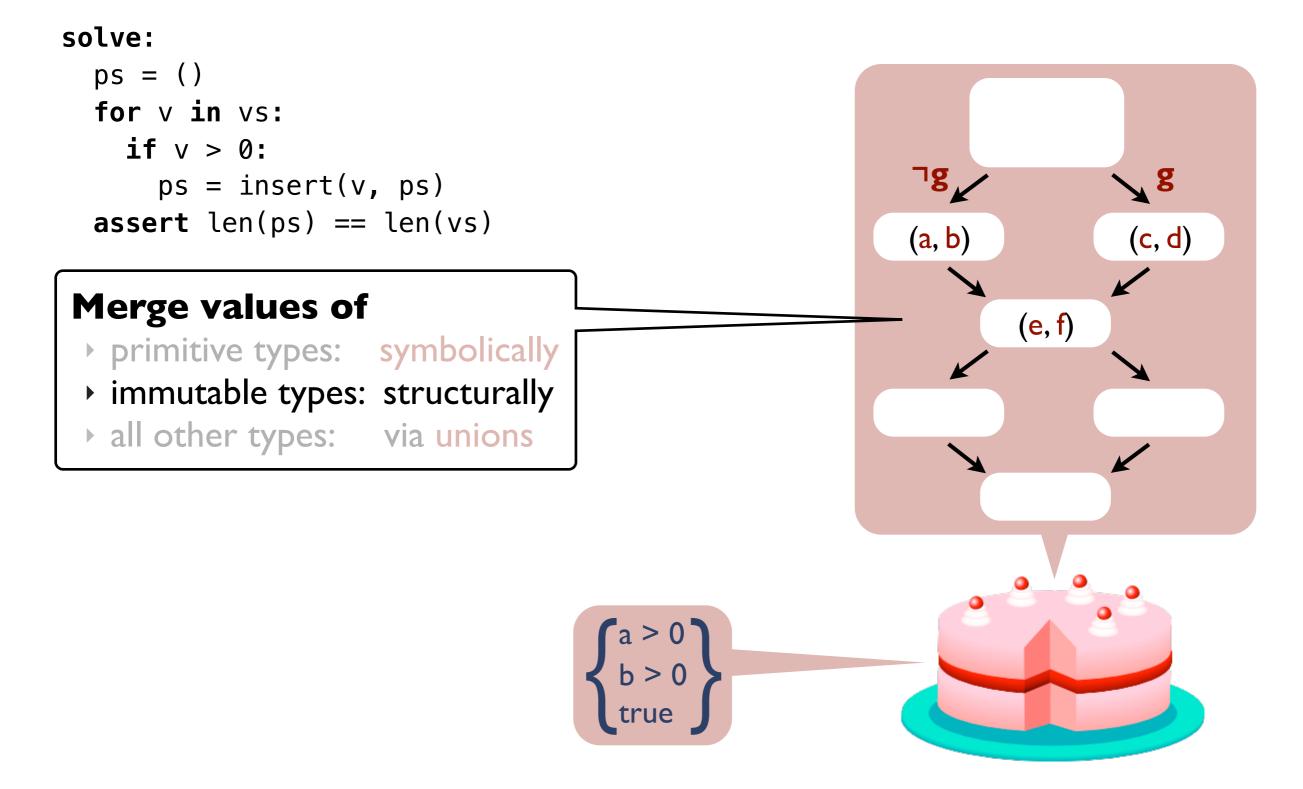
```
solve:
    ps = ()
    for v in vs:
        if v > 0:
            ps = insert(v, ps)
        assert len(ps) == len(vs)
```

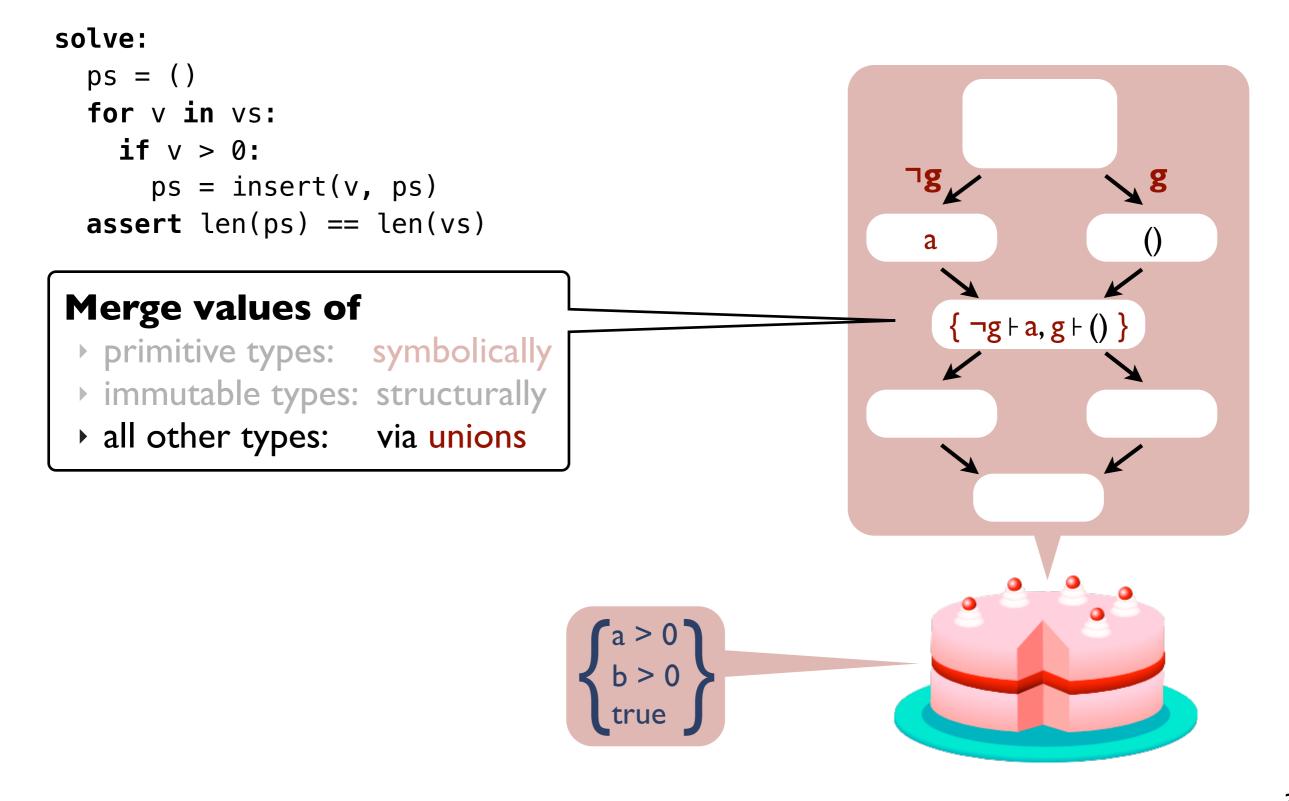




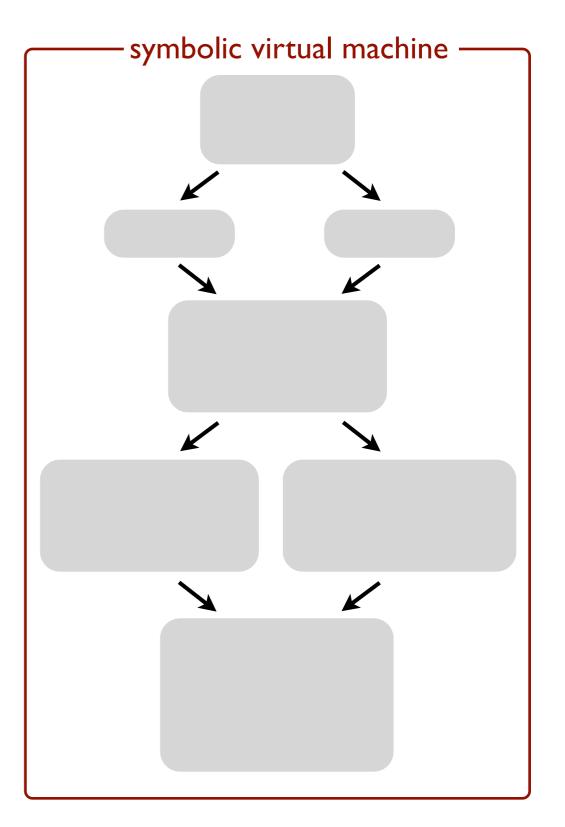
 $\begin{cases} a > 0 \\ b > 0 \end{cases}$



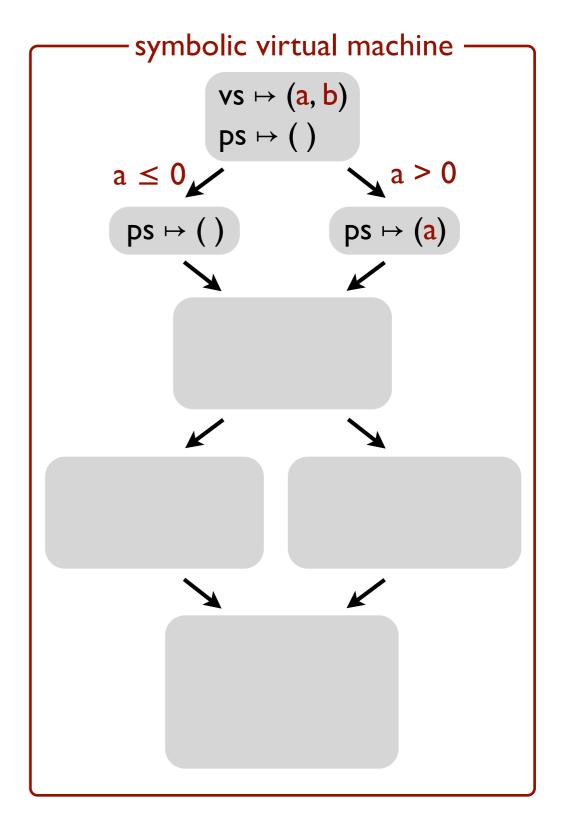


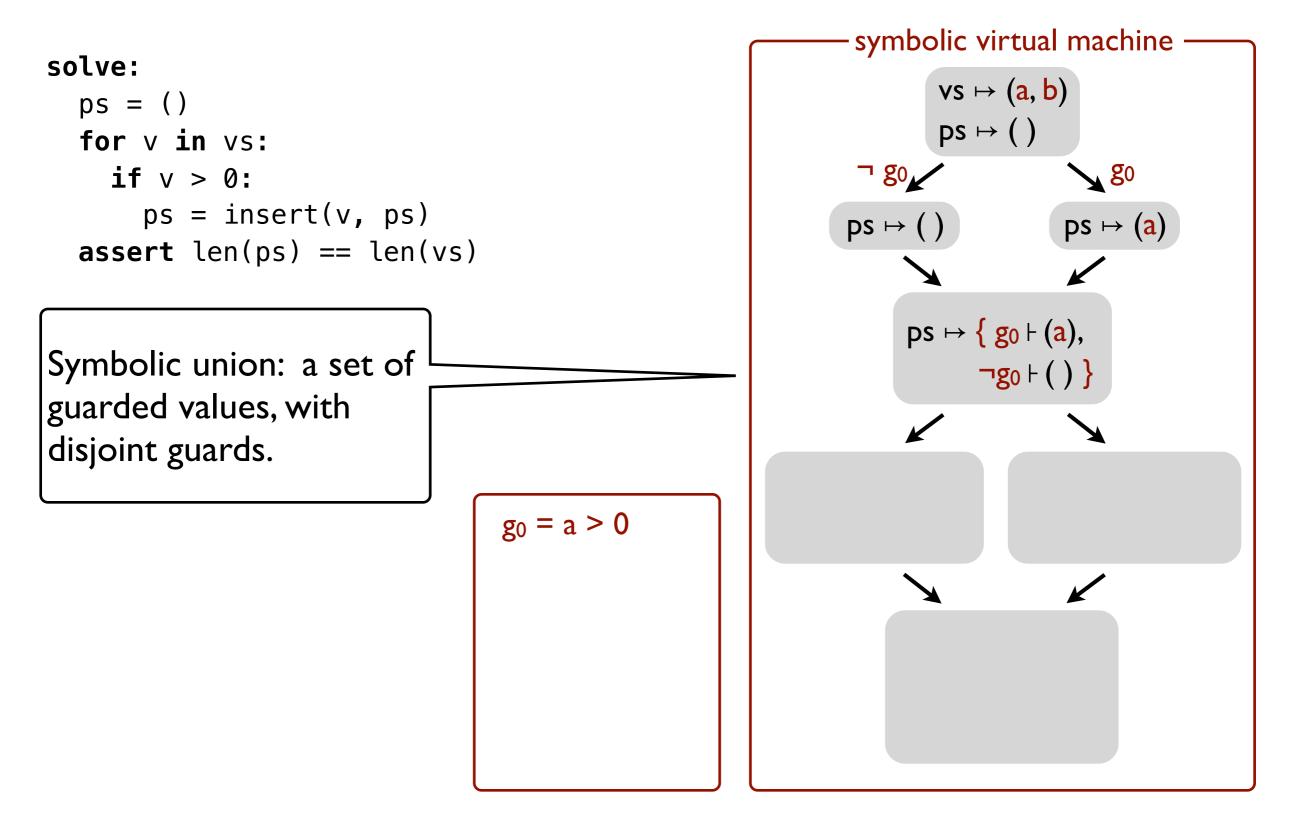


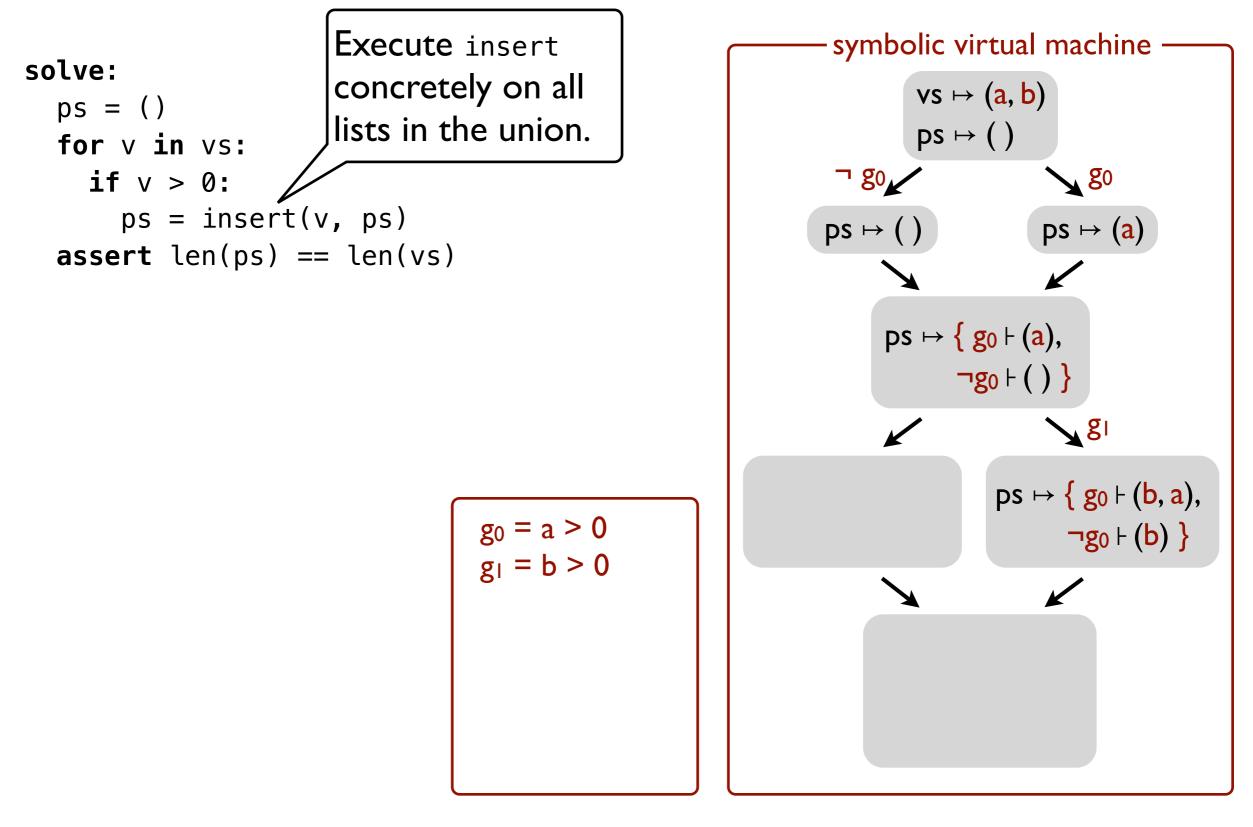
solve:
 ps = ()
 for v in vs:
 if v > 0:
 ps = insert(v, ps)
 assert len(ps) == len(vs)



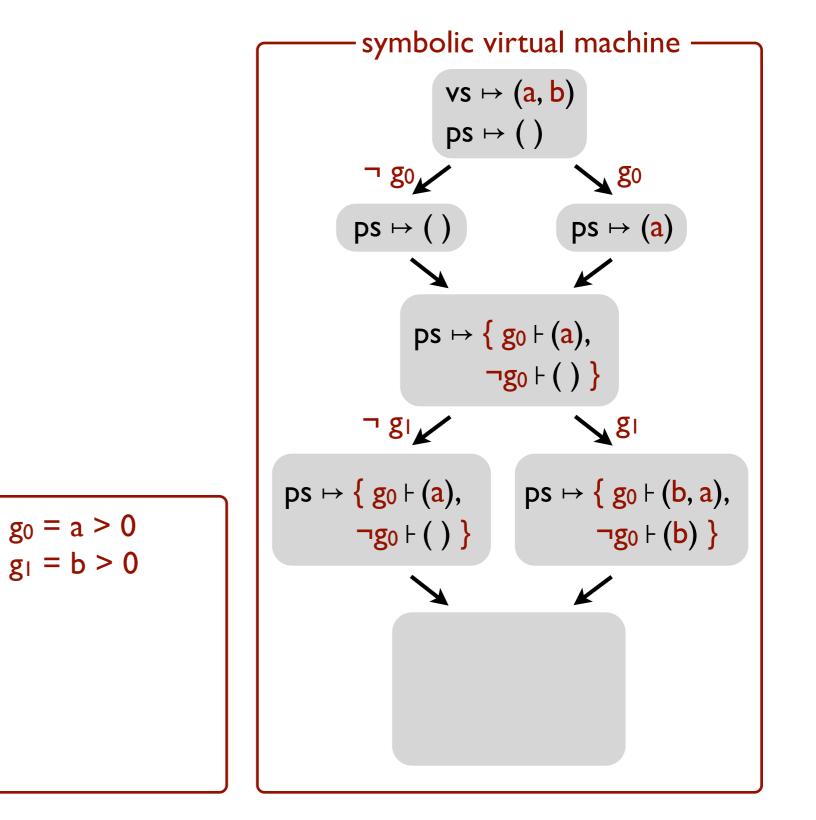
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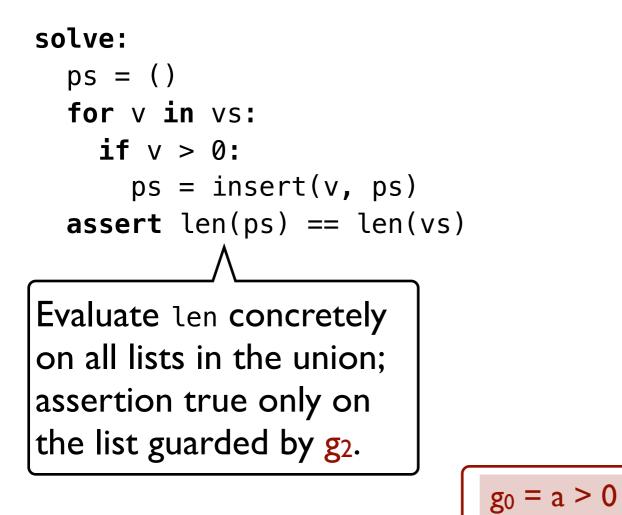
 $g_1 = b > 0$

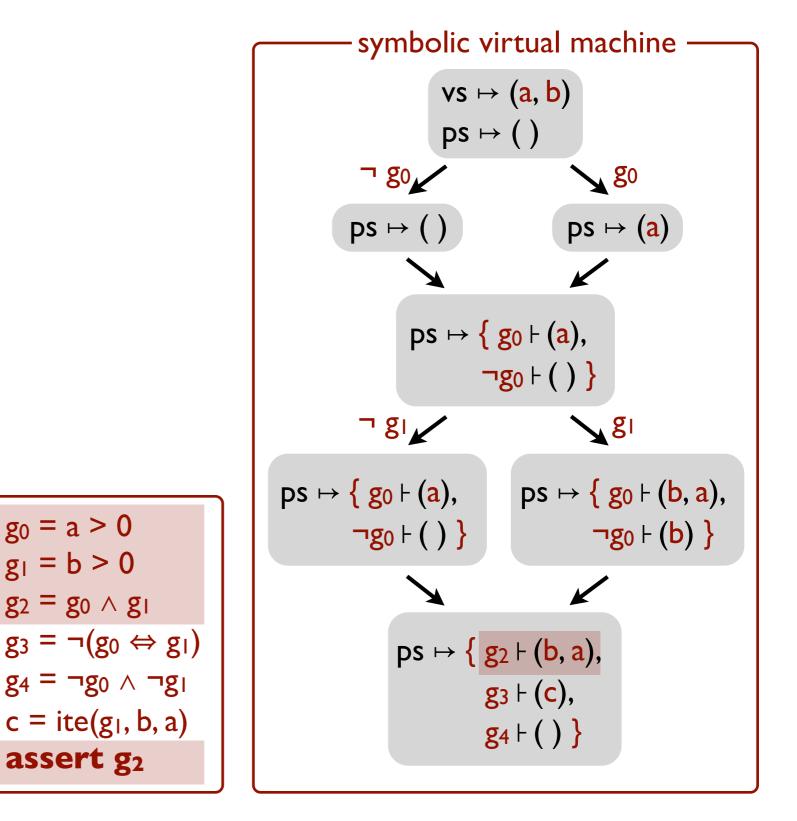
 $g_2 = g_0 \wedge g_1$

 $g_4 = \neg g_0 \land \neg g_1$

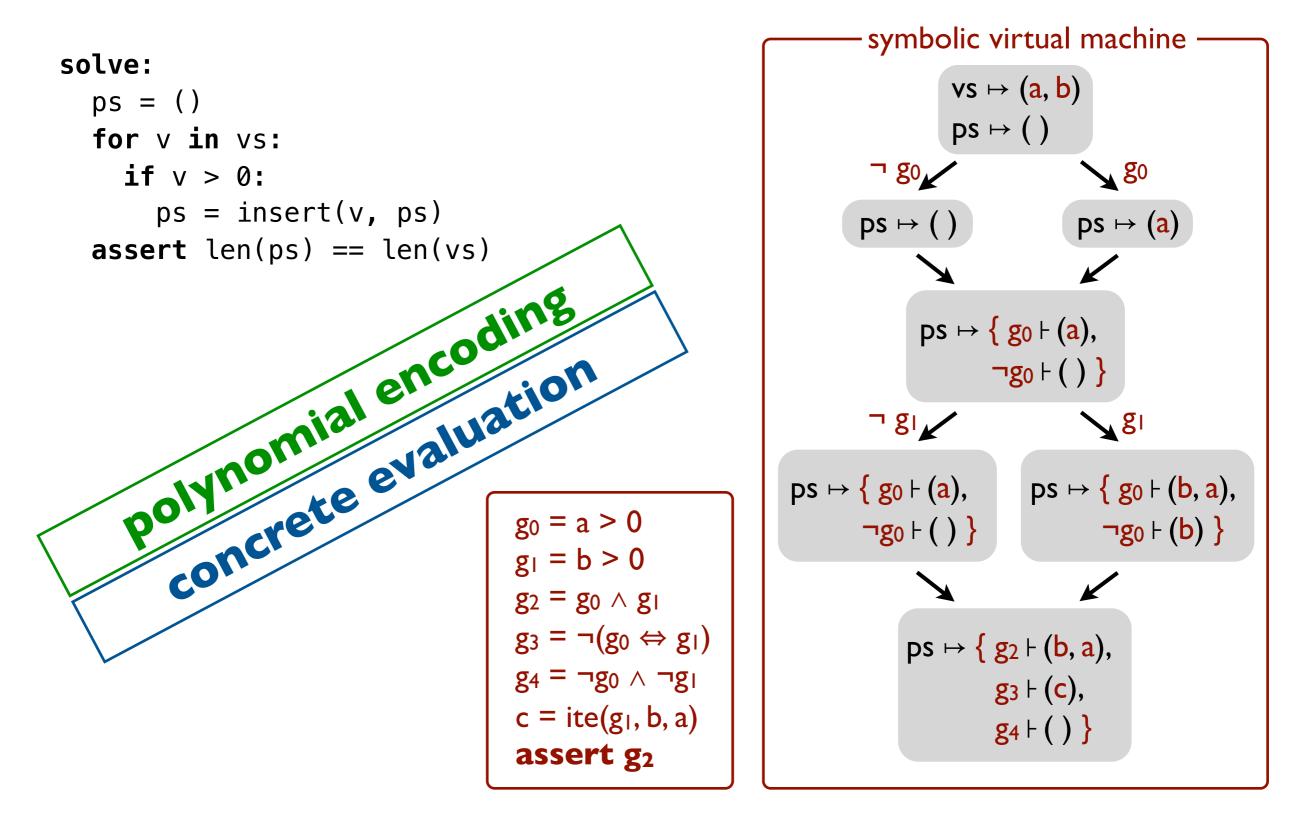
 $c = ite(g_1, b, a)$

assert g₂





A new design: type-driven state merging



How to build your own solver-aided tool



The classic (hard) way to build a tool

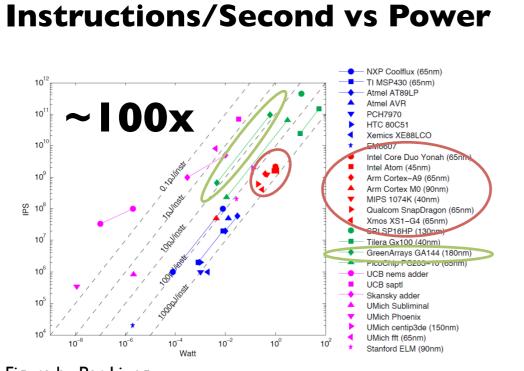
What is hard about building a solver-aided tool?

An easier way: tools as languages How to build tools by stacking layers of languages.

Behind the scenes: symbolic virtual machine How Rosette works so you don't have to.

A last look: a few recent applications

Cool tools built with Rosette!



GreenArrays GA144 Processor

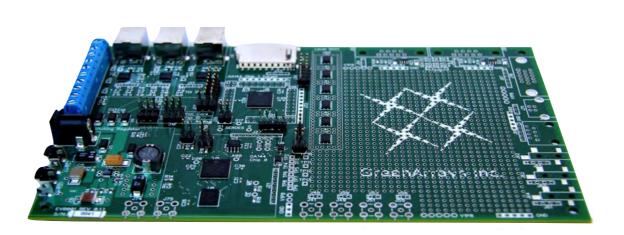


Figure by Per Ljung

GreenArrays GA144 Processor

- Stack-based 18-bit architecture
- 32 instructions
- ▶ 8 x 18 array of asynchronous cores
- No shared resources (cache, memory)
- Limited communication, neighbors only
- < 300 byte memory per core</p>

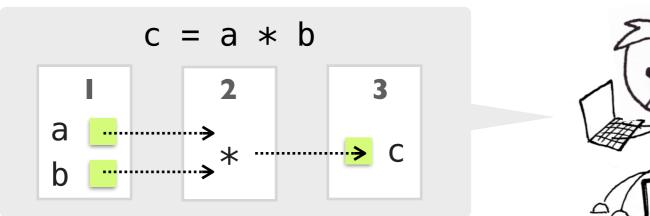
Manual program partitioning: break programs up into a pipeline with a few operations per core.



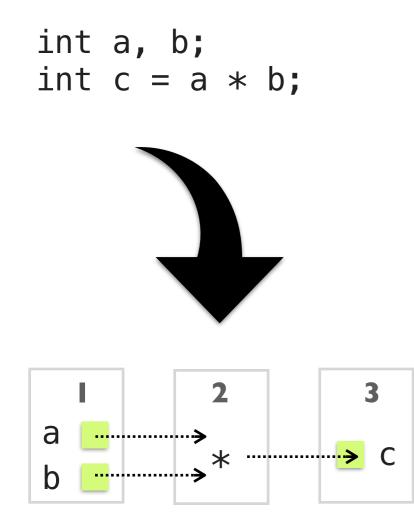
Drawing by Mangpo Phothilimthana

GreenArrays GA144 Processor

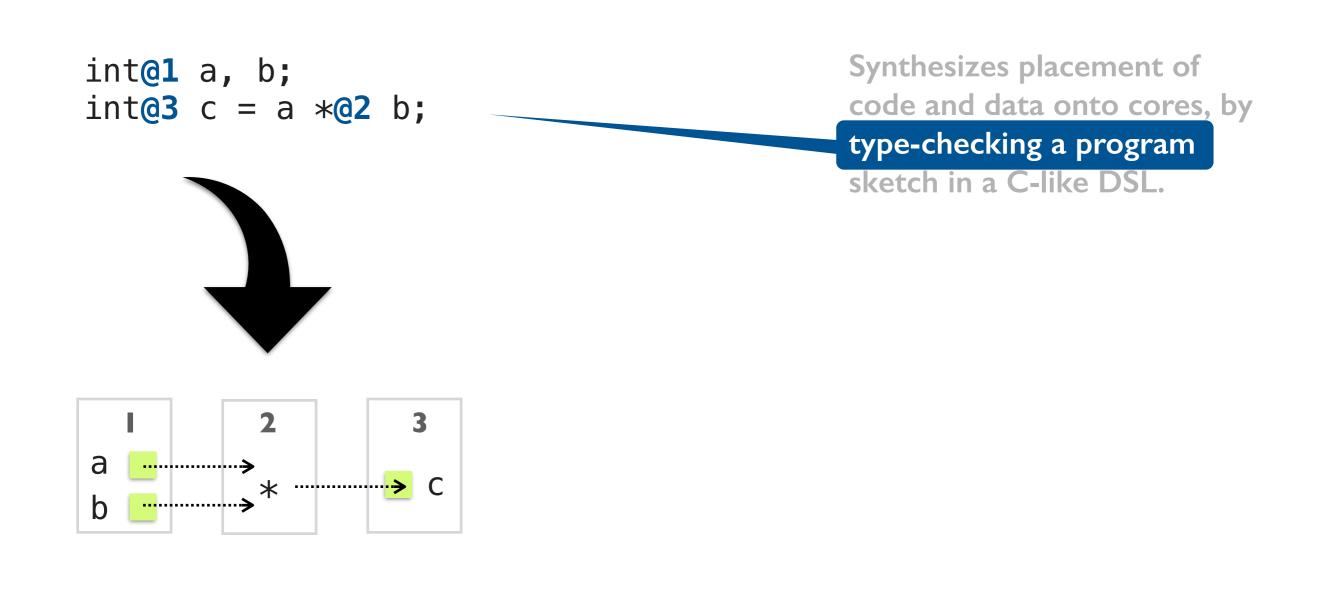
- Stack-based 18-bit architecture
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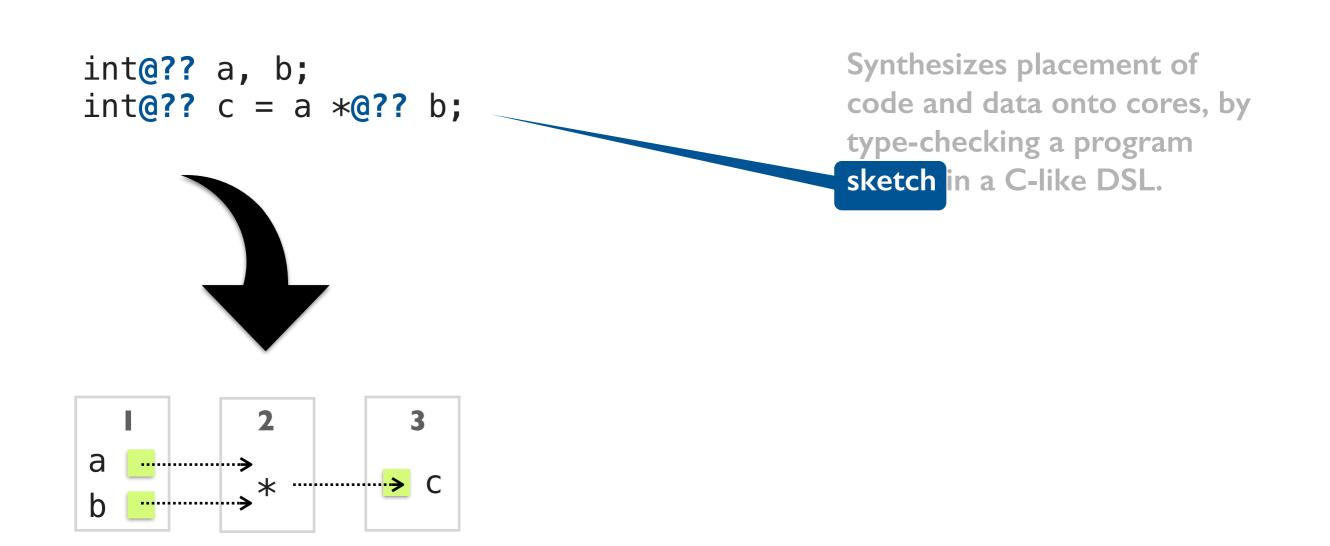


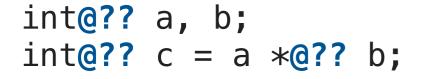
Drawing by Mangpo Phothilimthana

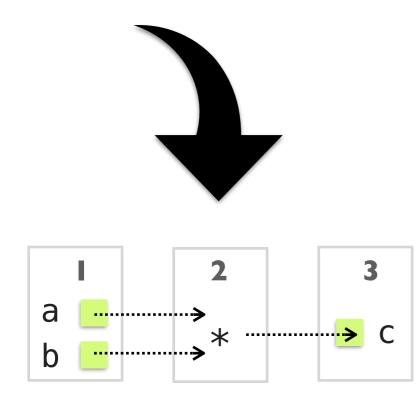


Synthesizes placement of code and data onto cores, by type-checking a program sketch in a C-like DSL.





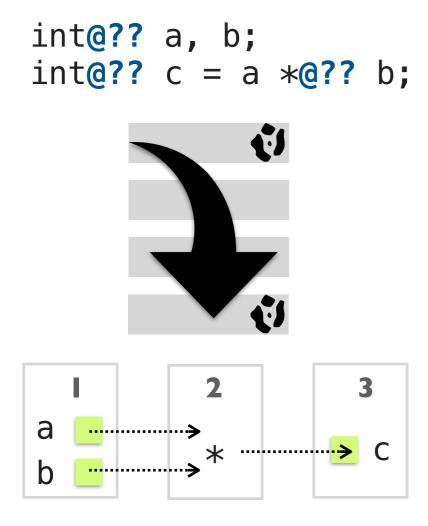




Built by a first-year grad in a few weeks



Phitchaya Mangpo Phothilimthana



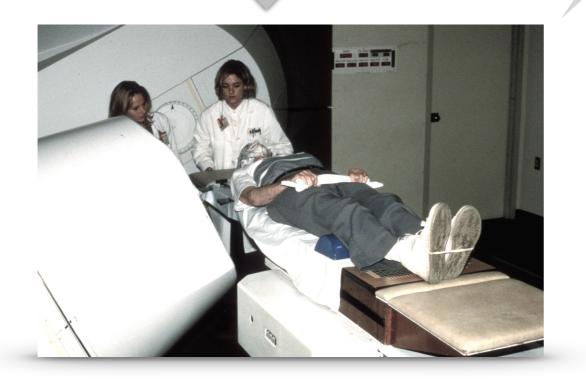
With Chlorophyll, it took one afternoon to build a set of apps that took 3 months to build manually.



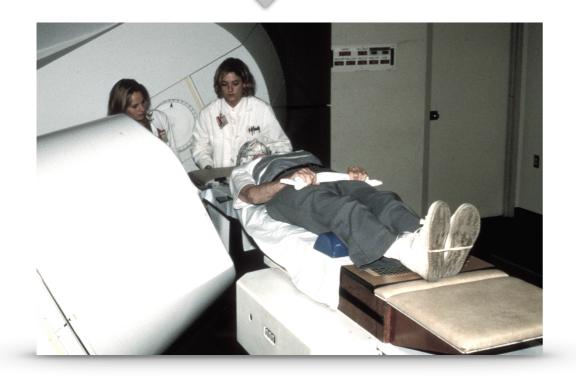
[Phothilimthana et al., **PLDI'I4**]

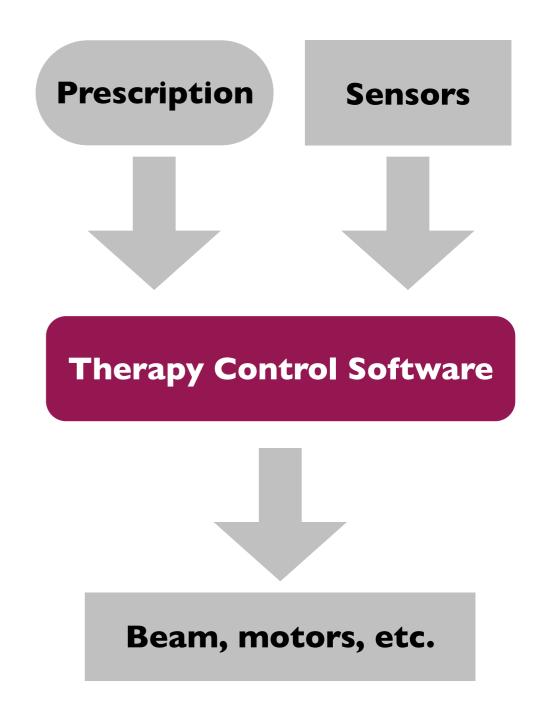
Clinical Neutron Therapy System (CNTS) at UW

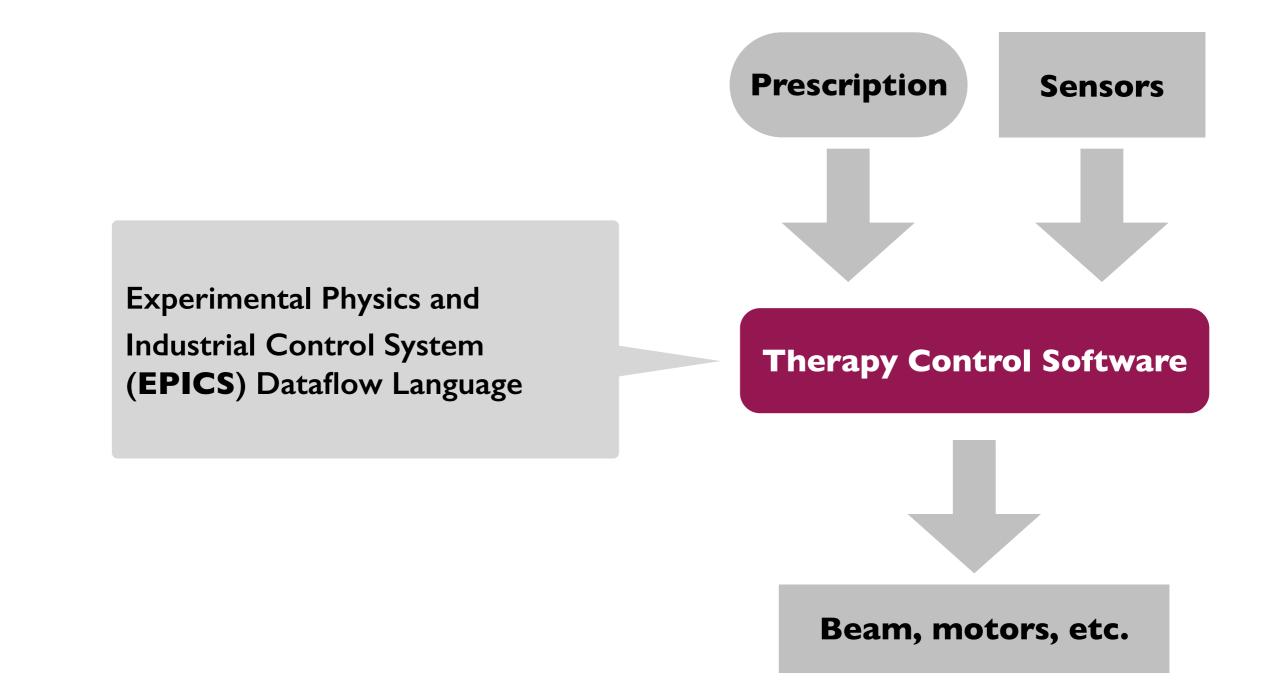
- 30 years of incident-free service.
- Controlled by custom software, built by CNTS engineering staff.
- Third generation of Therapy Control software built recently.



Clinical Neutron Therapy System (CNTS) at UW

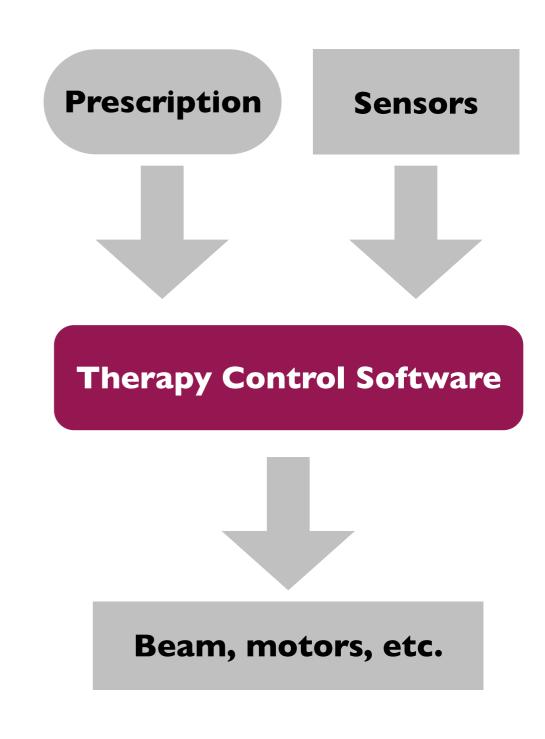


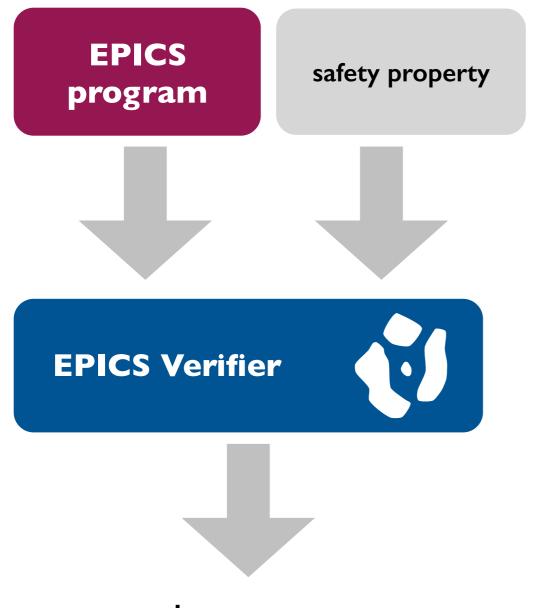




EPICS documentation / semantics

The Maximize Severity attribute is one of NMS (Non-Maximize Severity), MS (Maximize Severity), MSS (Maximize Status and Severity) or MSI (Maximize Severity if Invalid). It determines whether alarm severity is propagated across links. If the attribute is MSI only a severity of INVALID_ALARM is propagated; settings of MS or MSS propagate all alarms that are more severe than the record's current severity. For input links the alarm severity of the record referred to by the link is propagated to the record containing the link. For output links the alarm severity of the record containing the link is propagated to the record referred to by the link. If the severity is changed the associated alarm status is set to LINK_ALARM, except if the attribute is MSS when the alarm status will be copied along with the severity.



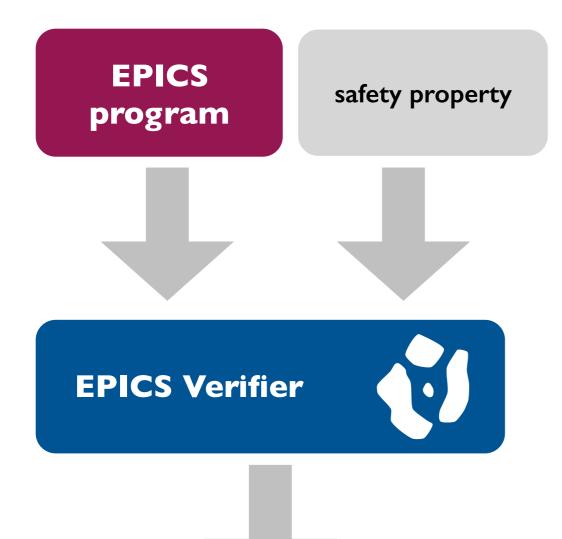


Built by a 2nd year grad in a few days

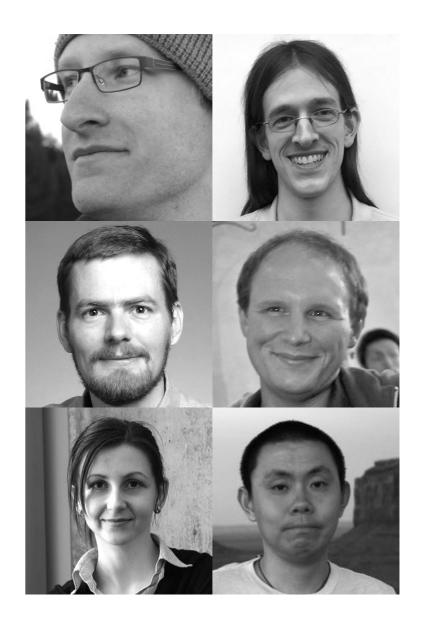


Calvin Loncaric

bug report

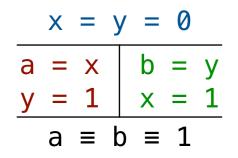


Found a bug in the EPICS runtime! Therapy Control depended on this bug for correct operation.

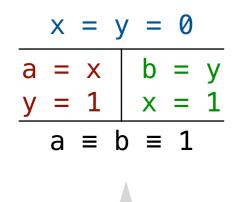


[Pernsteiner et al., CAV'16]

Memory consistency models define memory reordering behaviors on multiprocessors.



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Forbidden by sequential consistency.

Allowed by x86 and other hardware memory models.

Memory consistency models define memory reordering behaviors on multiprocessors.

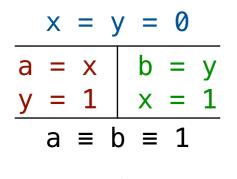
$$\begin{array}{c|c} x = y = 0 \\ \hline a = x & b = y \\ y = 1 & x = 1 \\ \hline a \equiv b \equiv 1 \end{array}$$

Forbidden by sequential consistency.

Allowed by x86 and other hardware memory models.

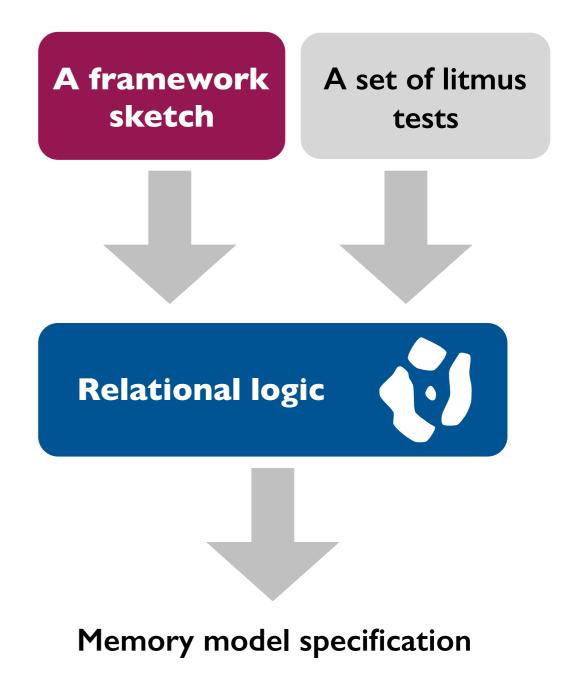
Formalizing memory models is hard: e.g., PowerPC formalized over 7 publications in 2009-2015.

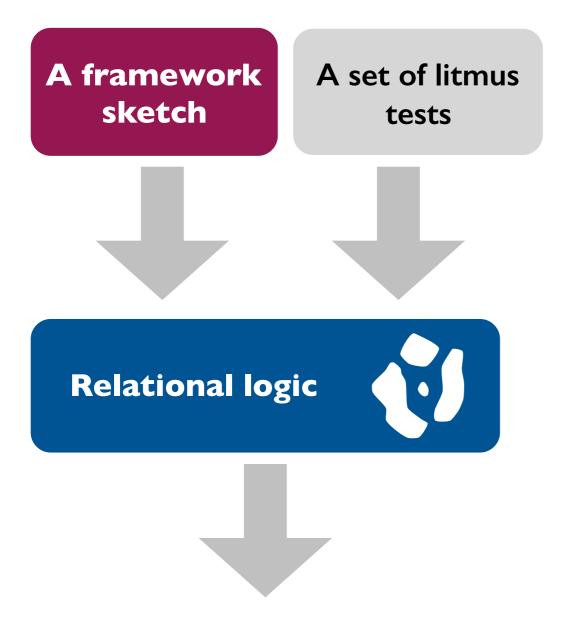
Memory consistency models define memory reordering behaviors on multiprocessors.



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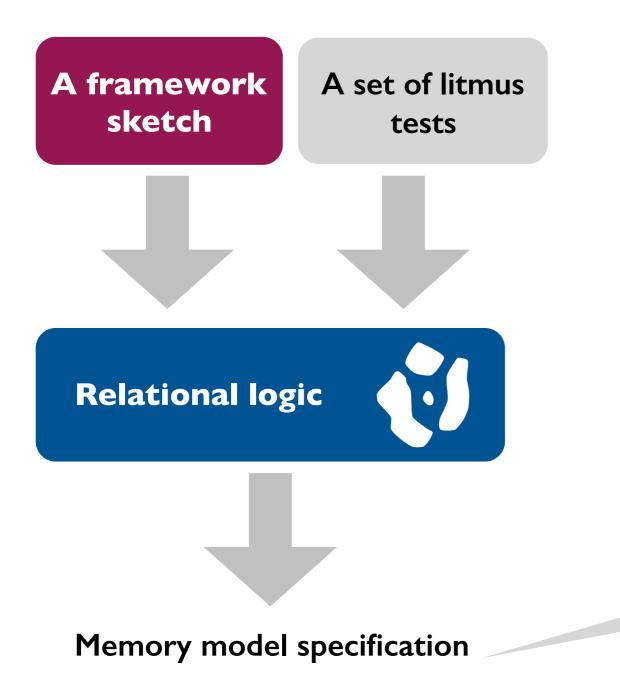


Built by a 2nd year grad in a few weeks



James Bornholt

Memory model specification





[Bornholt and Torlak, PLDI'I7]

Synthesized PowerPC in 12 seconds from 768 previously published tests. Synthesized x86 in 2 seconds from Intel's litmus tests. Discovered 4 tests are missing from the Intel manual.

Thanks for a great quarter!

