CSE471—Computer Design and Organization

Prof. Steven Burns *Autumn 1994*

Lecture Notes: 30th Day

Input and Output

- We must interface the processor to the outside world:
  - Keyboard and mouse
  - Graphic Displays
  - Networks
  - Disks and Tapes
- There is a great disparity is data transfer rates for these devices. There is also a disparity in the user's willingness to cope long latencies.

Busses

- Used to transfer data from the processor to various I/O devices (and to physical memory)
  - Processor–Memory — mostly proprietary
  - I/O — SCSI, GPIB
  - Backplane — VME, NuBus, SBUS, PC/AT
- Synchronous vs. Asynchronous
- One master vs. multiple masters

Interaction with Processor

- Polling
- I/O interrupts
- Direct Memory Access (DMA)
- Memory-mapped I/O
- Special I/O instructions

Cache Coherency Problem

- DMA transfers between main memory and the I/O device may be using stale data because a newer value in the cache may not have been updated to main memory, or may have been updated to main memory but not to the cache.
- Three techniques:
  - Route the I/O transfer through the cache.
  - Have the OS invalidate the cache on I/O reads and write back the cache on I/O writes.
  - Selectively invalidate the cache using hardware that snoops the bus traffic. (Used mainly in shared-memory multi-processors.)

NuBus — The Macintosh's Backplane Bus

- Simple synchronous bus
- Single large physical address space
- Only *Read* and *Write* operations supported
- I/O operations are memory mapped
- Small pin count — time-multiplexed data and addresses
- Distributed master arbitration

Signals

```
/RESET                         Reset
/CLK                           10 MHz Clock 75% duty cycle
/PFW                           Power fail warning
/NMRQ                          Non-master request

/START                         Start
/ACK                           Acknowledgment
/TM[1:0]                       Transfer mode

/AD[31:0]                      Address/data
```

`/ARB[3:0]`	`Arbitration`
`/RQST`	`Request`
`/SP`	`System parity`
`/SPV`	`System parity valid`
`/ID[3:0]`	`Slot identification`
`+5V`	`11 pins`
`+12V`	`2 pins`
`-12V`	`2 pins`
`-5.2V`	`8 pins`
`GND`	`22 pins`

NuBus Timing

- The system clock is setup to be high for 75ns and low for 25ns.
- The signals are sampled on the falling edge.
- The signal are driven in the 75ns interval before the falling edge.
- Skew problems are avoided by the 25ns dead interval.

Read Data Transfer

- For exactly one cycle, a *master* asserts (lowers) `/START` while driving `/TM` and `/AD`. These values determine the transfer mode and the physical address of the transfer.
- The addressed *slave* samples the `/TM` and `/AD` signals. The master waits for `/ACK` to be asserted.
- Some number of cycles later, again for exactly one cycle, the slave asserts `/ACK` and drives data on `/AD` and places a status code on `/TM`.
- If the slave fails do respond in $2 \leq n < 256$ cycles, a timeout occurs.
- The read bandwidth is 1 word per every 2 cycles, or 20 MB/s.

Write Data Transfer

- Master asserts `/START`, and drives `/AD` and `/TM`. The addressed slave samples the address.
- The next cycle, the master releases `/START` and `/TM`, but drives `/AD` with data. It continues to drive `/AD` until the Acknowledgment is received.
- Some number of cycles later, the slave asserts `/ACK` and drives the status code on `/TM`. On the next cycles, the bus can be used for another operation.

Status Codes

- `/TM` is set to one of four values when `/ACK` is asserted.
  - Bus transfer complete
  - Error
  - Bus timeout error
  - Try again later

Interrupts

- There is one global signal `/NMRQ` (non-master request) that can be pulled down by any of the slots. The processor can interrupt on this signal and then poll the slots to determine which slot wants attention.
- The Macintosh designer's didn't like this. They keep the individual `/NMRQ` lines around (like a Cause register) and bring them to the processor through an interrupt controller.

Block Data Transfer

- 2, 4, 8, or 16 words can be transferred with a single start cycle using block transfer mode.
- The master determines the size of the block, setting the `/TM` and low-order `/AD` bits appropriately.
- There is an intermediate acknowledge (`/TM[0]`) for every word transferred.

- The final assertion of `/ACK` ends the transfer.
- It is possible to transfer one word per cycle (actually 16 words in 17 cycles) in this mode. The resulting bandwidth is close to 40 MB/s.

Arbitration

- Multiple masters arbitrate for the bus. Arbitration takes two clock cycles. Slots may only request control of the bus if an arbitration is not in progress (helps achieve fairness.)
- To start an arbitration, the contending slots assert `/RQST` and attempt to change the signals `/ARB` using the equations:

```
/ARB[3] = /ID[3] & ARB
/ARB[2] = /ID[2] & ARB & (/ID[3] | ~/ARB[3])
/ARB[1] = /ID[1] & ARB & (/ID[3] | ~/ARB[3])
        & (/ID[2] | ~/ARB[2])
/ARB[0] = /ID[0] & ARB & (/ID[3] | ~/ARB[3])
        & (/ID[2] | ~/ARB[2]) & (/ID[1] | ~/ARB[1])
GRANT   = ARB & (/ID[3] | ~/ARB[3])
        & (/ID[2] | ~/ARB[2]) & (/ID[1] | ~/ARB[1])
        & (/ID[0] | ~/ARB[0])
```

- The `/ARB` signals are all open-collector.
- After a short delay, `/ARB` will equal `/ID` for the highest priority slot that participated in the contest.

Bus Locking and Bus Parking

- Bus locking — To do critical tasks, slots can lock the bus for multiple cycles. In this case, the slot continues to assert `/RQST`. Software control of the floppy disk and implementation of Test-And-Set instructions are examples where locking is helpful.
- Bus parking — After an arbitration, the winning master maintains control of the bus until a new winner is determined and the current bus transaction is completed.

SCSI

- Small Computer System Interface
- Parallel, multiple master (peer-to-peer), I/0 bus
- Actually used in large computer as well as small. (Actually the name was a good political decision. They got ANSI standardization without having to compute against designs targeted toward large computers.)
- Can support 8 devices, each with 256 logical subunits.
- Two electrical flavors: single-ended, differential.

Details

- Bi-directional data originally on 8 wires.
- Competitors used uni-directional wires because of channel turnaround time was too great to finely control the operation of a fast disk drive.
- SCSI solves this by putting more intelligence in the disk drive itself.

Phases

- BUS-FREE
- ARBITRATION
- SELECTION
- RESELECTION
- COMMAND
- DATA
- STATUS
- MESSAGE

Wires

- SE: 18 signal wires, 30 GND, 1 TERMPWR, 1 empty
- Diff: 18 signal pairs, 11 GND, 2 TERMPWR, 1 DIFFSENS

```
ACK    Initiator acknowledgment to data transfer
ATN    Initiator asks for a message from the target
BSY    Bus busy
C/D    Control or Data
DB[7:0],DBP  Data lines and data parity
I/O    Data transfer direction relative to initiator
MSG    Message on bus (controlled by target)
REQ    Target requests data transfer
RST    Reset bus
SEL    Data lines hold ID information
```

Performance

- SCSI-1: 2 MB/s asynchronous, 4 MB/s synchronous
- SCSI-2: up to 10 million transfers/s of up to 4 byte =¿ 40 MB/s
- To get the high speed, the initiator and target must negotiate.