Answer sheet for the review

1. The data on predicting branches using data on the most recent n branches:

n	Compiler	Business	Scientific	OS
3	93.7	96.6	91.0	83.5

so the percentage is 93.7% * 10% + 22% * 83.5% + 91.0% * 68% = 89.95%

2. Expected Delay = 0.8*(1-0.402)*0+0.2*(1-0.402)*5+0.2*0.402*4+0.8*0.402*0 = 0.9196

Double cache makes delay = (1-0.636) * 0.2 * 5 + 0. 2* 0.636 * 4 = 0.8728

3. The two bits that form ALUOp are RegDst and Branch. RegDst is 1 for arithmetic operations where the function field (Offset bits are the other input) determines the operation. Branch is 1 if the instruction is a branch operation, else 0. These settings are created whenever Op changes.

4. The #(32) here means the bit-width of the register is 32. (actually it sets the parameter width of enreg to be 32)

5. _with_clear means the register has a control bit which could reset the register value to be 0.

6. Yield is the number of good chips that results from a wafer. When area increases fewer fit on a wafer and there is a greater probability that a defect will ruin the chip.

7. false. actually 4 times as many transistors fit on a chip since when feature size is reduced by one half, the area is reduced by 4 times. (square of size).

8. It's a dimensionless length defined in a chip design to accommodate the scalable property.

9. 32 * 32 *2 + 32 * (32+2+10) * 0.6 =

10. Pins are basically the input/output hardware which makes up the interface between different function hardware modules. Since pins are few so they should be wisely used. When working on vectored caches they usually do multi read/write instead of one such step to finish the operation.

11. 3 C's in cache misses are capacity miss, compulsory miss and conflict miss.

12. It's an open question.

13. 4 * 32*512 = 64 KB bytes

14. benefits: make best use of cache size

Liability: expensive, slower than other cache.

15. benefit: cheap, fast

liability: cause more conflict

16. In the colored pages scheme, we suppose the OS chooses pages so that the LSB of the tag portion of the virtual address matched the physical address, so this color bits method could make more untranslated bits to be used to address the cache. we can devise many other ways to increase the bits used to address cache, for instance, we can increase the set column, and the cache size.

17. A write through cache typically will not allocate on write since it simply goes to the memory and writes the byte that doesn't reside in the cache to the memory.

18. every entry of a cache needs 2 bits, so in all

2 * 4 * 512 = 4096 bits

19. False. Actually it can only achieve 3-4% better miss rate and a rule of thumb is that any n-associative scheme with n>4 won't make any significant improvement in terms of miss rate.

20. In general the requirement is Compatible. So we have to make sure

L2 line >= L1 line

L2 sets >= L1 sets

L2 associativity >= L1 associativity

L2 size/(L2 assoc * L2 line size) >= L1 size / (L1 assoc * L1 line size)

L2 size/L2 assoc >= L1 size/L1 assoc * (L2 line size/L1 line size)

L2 should be substantially larger than L1.