CSE471 A96 Snyder

20 Questions

1. A processor plans to use a 2 bit saturating counter to strore branch histories for branch prediction. The load is 10% compilation, 22% operating system and the remainder is scientific programs. What percentage of the branches are expected to be correctly predicted?

2. A BTB requires 8 bytes for each entry (4 for the address, 4 for the target address; ignore counters). Assuming a complete scientific workload and a 64 byte BTB, what is the expected delay for branches? Suppose the table size is doubled, what is the improvement?

3. It appears that the `alucontrol` routine module does not have the instruction opcode as an input. How does the `mips` behavioral simulator know what instruction is being executed?

4. What does the "`#(32)`" mean in the instruction:

```
enreg #(32) id_ex_wreg_3( clk, 1'b1, id.offset, ex.offset);
```

5. What does the "`_with_clear`" mean in the instruction:

```
enreg_with_clear #(9) id_ex_wreg_6( ... );
```

6. If a die for a processor chip is increased in area, the yield will go down. What is the "yield" and what are the two reasons that it goes down?

7. If the feature size of a chip technology is reduced by half, twice as many transistors fit on a chip. True or False? Explain.

8. What is λ in VLSI techology?

9. Estimate for a 32 entry BTB how much silicon area it is likely to occupy in **rbe**s.

10. What are "pins" and how are they related to sectored caches?

11. What are the 3 "C's" of cache misses?

12. Three reasons were given in lecture for programs to exhibit locality. Can you think of any more?

13. A 4-way set associative cache with line size 32B and 512 sets contains how many bytes of data?

14. What are the benefits and liabilities of a fully associative cache?

15. What are the benefits and liabilities of a direct mapped cache?

16. What problem are color bits trying to solve for caches? Explain other ways that this problem can also be solved.

17. A write through cache typically will/will not allocate on write? Explain.

18. For the cache in question 13, how many bits will be needed in the entire cache to implement LRU line replacement?

19. True or fale: A fully associative cache will typically have a 10% better miss rate than a 4-way set associative cache.

20. What is required for the inclusion property ot hold between an L2 and L1 cache?