Class -- here is a quick brain dump of this morning's midterm, which I haven't even proof read or checked. I thought you might want to check your answers.
-- LS

1. [15] Short explanations:
(a) In 2's complement binary addition, overflow is not possible when the signs of the operands are opposite because *the result must be somewhere in the numerical range bounded by the two operands, and thus representable.*

(b) Unconditional register branches (BRR, BALR) typically require fewer pipeline stalls than their "computed address" counter-parts because *computing the address, which can involve two adds (two registers and an offset) is not necessary, and so the target instruction fetch (TIF) can be initiated earlier.*

(c) The instruction run length for VAX programs is shorter than the run length for MIPS programs because *the encoding of VAX (an R+M architecture) instructions is denser than is the MIPS encoding, leaving fewer instructions to make up a run.*

(d) A biased exponent is *the standard representation of the exponent in floating point numbers wherein the upper half of the unsigned numerical range is assigned positive, and the lower half is assigned negative; the biased exponent minus the bias yields the actual exponent.*

(e) The Alpha21264 L/S architecture can issue 4 instructions per clock tick and can do two 64-bit loads or stores to its I-cache per clock tick. For instructions of length ___32___-bits, this is perfect *because the number of instruction bits needed per tick (4*32) equal the number fetched (2*64).*

2. [5] The following op-codes come from the program segment in question 4.
(a) mark the ends of each instruction run with a vertical line:

```
LD  LDA  MOVE  CMP  BC | AND  BCT | MPY INC SHR  BR | BRR |
```

(b) What is the average run-length for this program segment? *12/4=3*

x. A typical condition code is composed of 4 bits. (a) What is the meaning of each bit:

Bit	Meaning
0	*ALU result is positive*
1	*ALU result is zero*
2	*ALU result is negative*
3	*ALU result overflowed*

(b) Interpret the bit string 1010 in your assignment in part (a).
In this representation 1010 is not equal to zero.

4. [12] For each of the following instructions, indicate whether there are any features of the instruction that would affect its pipelined execution. [This is the 3N + 1 program.]

```
1.TNP1: LD.W      R4,N       ;Get oper      none
2.      LDA       R5,3[R0,R0];Load 3        none
3.Conv: MOVE      R6,R4      ;Put in tmp    data depend. on #1
4.      CMP.W     R6,One     ;Converged?    data depend. on #3
5.      BC.EQ     Done       ;If yes, qt    CC depenend on #4
6.EOtst:AND.W     R6,One     ;Clear all     data depend. on #3
7.      BCT       R6,Halv    ;Is number     delay computing B target
8.Tripl:MPY.H     R4,R5      ;Form prod     none
9.      INC       R4         ;Bump resu     data depend. on #8
10.Halv:SHR.W     R4,1       ;Divide by     data depend. on #9
11.     BR        Conv       ;Check for     branch target fetch
12.Done:BRR       R15        ;Return to     branch target fetch
13.One  WORD      #1d        ;Constant 1
        End
```

x. An astronomy program (that simulates the universe) is being executed on a MIPS R2000-like computer as described in another problem. It contains a 100 instruction sequence made up of 72 floating point operations, 5 of which are 15 EX cycle divide instructions and 2 of which are 33 EX cycle square root instructions. Assuming no other pipeline stalls in this sequence except the run-on instructions, what is the CPI for this sequence?

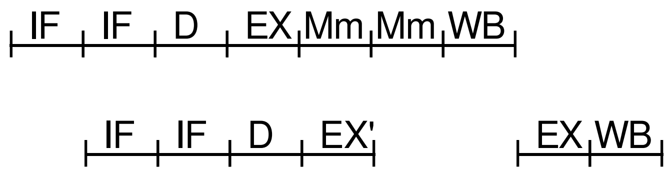
*(93*1 + 5*15 + 2*33)/100 =*

x. The timing diagram for the MIPS R2000 (studied in CSE378) assuming that cache reference time is 2 clock cycles is as follows:

IF	IF	D	EX	Mm	Mm	WB

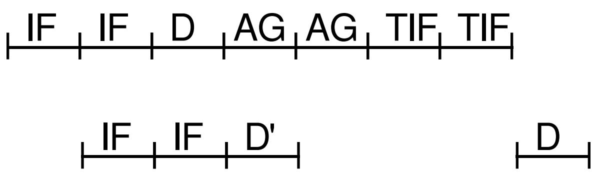
Evaluate the timing template for the instruction pair

```
l w   $4, Aarray ; Get array base
addi  $4, 4      ; Offset it by 4
```



x. Given the timing template for a R/M architecture,

(a) complete the template if the next instruction is an unconditonal branch (BR), i.e. show the execution of the BR and the instruction following:



(b) What is the pipeline delay for this branch? *4*

8. [3] The Alpha processor (Question 1e) has a 500MHz clock, giving it a peak execution rate of 2 giga instructions per second (GIPS), and a peak CPI of 0.25. Suppose that the CPI for instructions on this processor is actually 4.0 for typical programs. How many operations per second does it actually execute?

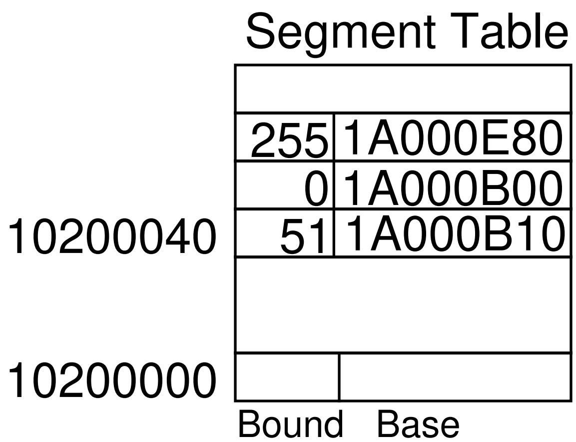
500MHz/4 CPI =125M Instructions/second

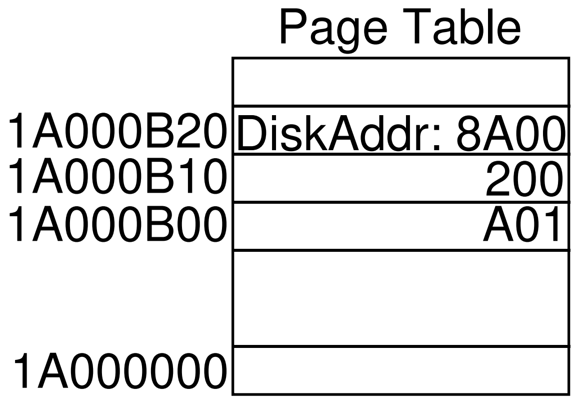
9. [5] Given the following information, translate the virtual address into its associated physical address.

Virtual Address			
	001	00	444

User ID	
	10200040

Physical Address		





Add the VA segment number (001) scaled by 4 to the user ID topoint to 0 1A000B00 which is the bound and base of thepage table for this segment. Add the page table number from the VA (00) to this base to get the page entry containing the high order bits A01. Append the page offset from the VA (444) to produce the address: 00A01444.

10. [0] My favorite Stone Temple Pilot is: Ò Eric Kretz, Ò Scott Weiland, Ò Robert DeLeo, Ò Dean DeLeo, or X *none of the above ... I prefer Pearl Jam?*