Shared Memory Multiprocessors

Also called symmetric multiprocessors (SMP)

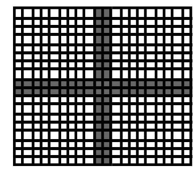
The basic idea is that multiple processors cooperate to execute a single program (parallel processing), by keeping their memories coherent.

Programming

A parallel program postulates multiple "threads" executing on the same data to solve a single problem.

Thread = PC + register state.

Producing a parallel program, both the writing and the compiling, are extremely interesting topics, but not our topic.



A
(4 processor decomposition)

ZPL

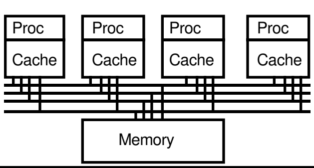
```
[1..n,1..n] repeat
              T := (A@n+A@e+A@w+A+@s)/4;
              err:= max<<(abs(A-T));
              A := T
            until err < 10^6;
```


Shared-bus Multiprocessors

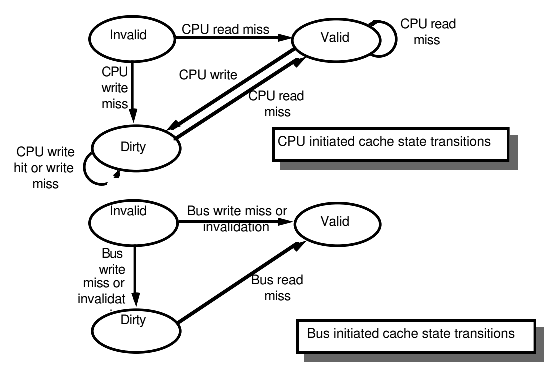
The (RAM) memory bus is expanded to host multiple processors. Each processor references its own cache in the usual way (assume 1 level of caching).

The contents of the caches are managed so that ALL processors see the same memory state.

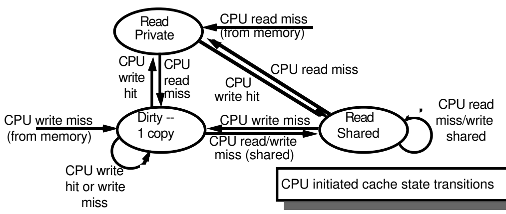
- If a processor writes to a cache line, any other cache containing that line will get the new value on its next reference
- The mechanism is called "snooping", since each cache can be aware (snoop) on the bus activity.



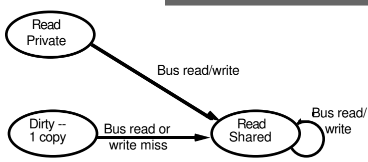
Write invalidate protocol



Firefly Protocol (Write-update)



CPU initiated cache state transitions



Bus initiated cache state transitions