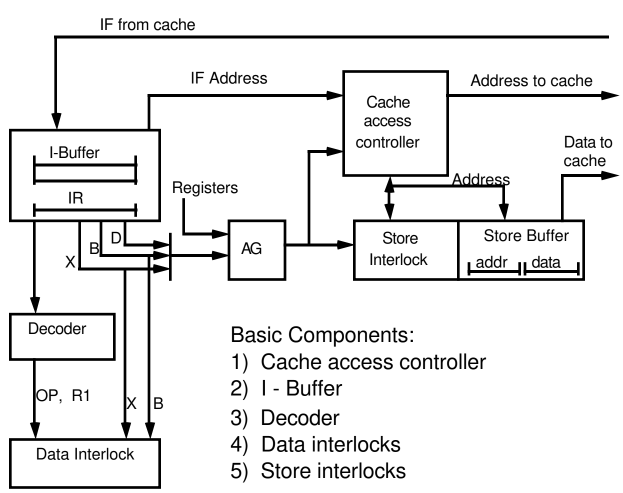
A Pipeline Design

We begin by focusing on the processor control, since the arrangement of the datapath parts tends to be direct.

Processor Control Unit



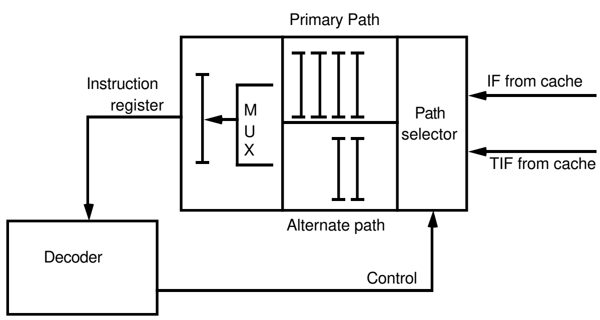
Basic Components:
1) Cache access controller
2) I - Buffer
3) Decoder
4) Data interlocks
5) Store interlocks

Instruction Buffering

Though indicated in the timing template as occurring prior to each decode, instruction fetching is usually batched and performed speculatively.

This *prefetching* with buffering assures that instructions are available, and the impact of instruction fetch on cache traffic is minimized.

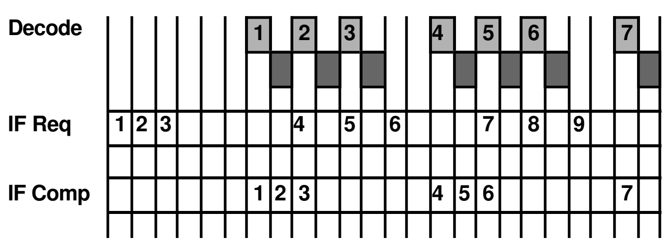
Runout -- condition of not having prefetched instructions



Prefetching

Prefetch registers are usually designed as circular buffers.
Multiple instructions, e.g. 2, are fetched together

3 Prefetch registers
6 ticks memory access
2 Instruction fetch



Buffer words = 1 + ceil(IF access time / Instructions-per-fetch)