Highlights from Chapter 2

- Flynn covers a variety of prelimiary topics in Chapter 2. Some, such are code density, are just not that important to us, while others, such as a $100M processor design study are not part of our curriculum.
- The issues having to do with silicon density, yield and cost are relevant.

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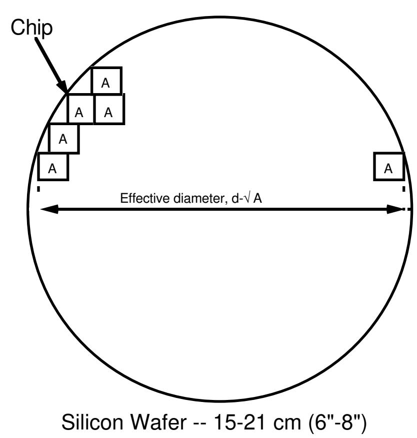
Silicon -- The Substance of Computers



Chips per wafer:

$$N = \frac{\pi(d-\sqrt{A})^2}{4A}$$

Silicon Wafer -- 15-21 cm (6"-8")

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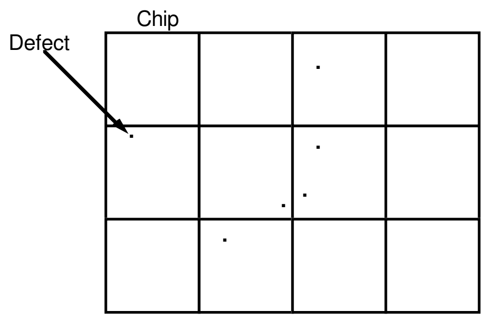
Defects in Fabrication



N_G = number of good chips

N_D = no. wafer defects

ρ_D = defect density per unit area

$N_D/N = \rho_D A$

$Yield = e^{-\rho_D A}$

Die cost is incurred in two ways. The larger the die the fewer that fit on a wafer. Further, the larger the die the more likely it is defective.

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Computing Cost of Die

Let a 21cm wafer cost $5000 to fabricate. Compute the cost of the each functional die for 2.3cm and 1.0cim given a defect density of ρ_D=1 defect/cm^2

$N = \dfrac{\pi(d-\sqrt{A})^2}{4A}$ $\quad$ $N = 130$ for $A = 2.3$ $\quad$ $N = 314$ for $A = 1.0$

$Y = e^{-\rho_D A}$ $\quad$ $Y = 0.1$ for $A = 2.3$ $\quad$ $Y = 0.37$ for $A = 1.0$

$N_G = NY$ $\quad$ $130 \times 0.1 = 13$ $\quad$ $314 \times 0.37 = 116$

\$5000 / 13 = \$385 $\quad$ \$5000 / 116 = \$43

$\therefore$ *Area costs!*

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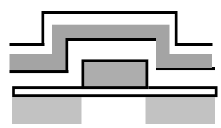
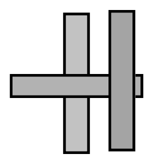
Silicon Design

Silicon technologies are specified by their minimum feature size, e.g. 0.5m, which is usually the length of a polysilicon gate (transistor), and the type(s) of field effect transistors used, CMOS = complementary metal-oxide-semiconductor devices, which include both p-channel and n-channel FETs.

Chip design is performed using a dimensionless length λ = the distance a feature of one layer can stray from another.

The minimum feature size $f = 2\lambda$





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Estimating Density of Components

Adopt a standard unit: register bit equivalent (rbe)

Roughly, the rbe = 2700 λ

Let f = 1μ
A = unit area = $f^2 \times 10^6$
1A = 1481 rbe
32 3-ported register file
= 32$\times$32 bits + sense & control
= (32 +6) $\times$ (32 + 6)
= 1444 rbe = 0.975A

Item	Size in rbe
1 register bit	1.0 rbe
1 static RAM bit (cache)	0.6 rbe
1 CAM bit (cache direct.)	2.0 rbe
1 DRAM bit	0.1 rbe

4KB direct mapped cache with 16 byte lines and 24bit tags

Data bits	= 4096 $\times$ 8 = 32,768
Tag bits	= 4096/16 $\times$ 24 = 6144
Cache size	= 195 + 06(32,768 + 6144)
	= 23,542 = 15.9 A

Take Home:
Silicon scales quadratically!
f/2 implies density$\times$4

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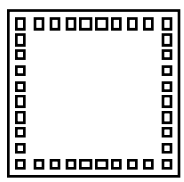
Pins and Pads

An integrated circuit encapsulates a lot of complexity, but ultimately it must attach to other circuits through I/O pins.

The density of I/O pads does not scale with the silicon technology, since it is determined by pad bonding mechanics.

To keep power and ground stable, aggressive chip designs must devote many pins to Vdd and Gnd, often more than are devoded to useful signals.

The best designs minimize the number off chip wires needed.



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