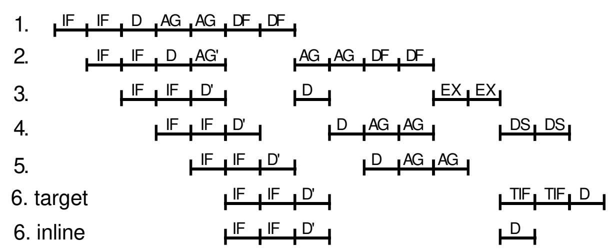
Five Instructions

```
1. LD     R7, 1000[R9,R8]
2. LD     R6, 1004[R10,R8]
3. SUB    R6,R7
4. ST     1008[R9,R8],R6
5. BCNE   24[R15,R14]
```

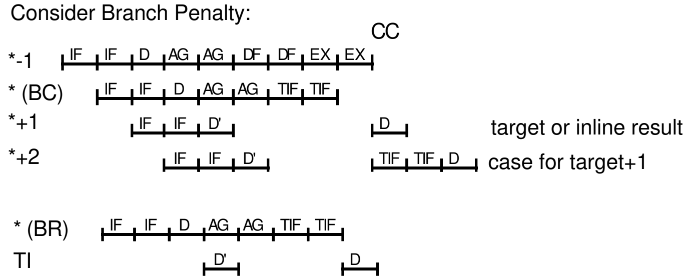
Inst	Dependency	Marg. Delay	Total Delay
1	none	0	0
2	address	3	3
3	data	0	3
4	none	0	3
5	(branch)	5	8
6	(no branch)	3	6



Computing CPI

CPI = 1.0 + $\Sigma\, w_i d_i$

Consider Branch Penalty:



For R/M architecture, 15% of instructions are branches (p.146). Of these, 20% are branches, 43% are branch on condition to target, and 37% are branch on condition, in-line.
CPI = 1 + 0.15*(5*0.37 + 5.5*0.43 + 4*0.2) = 1.75225

Early Condition Code Testing

Compiler moves CC setting instructions earlier in the program in order to give time for the CC to be set.

Revise branch delay based on the number of instructions interposed between CC setting and CC branching instructions.

n=0 implies no instructions interposed

For branches taken, revised delay is greater of n and unconditional branch delay.

	n=0	n=1	n=2	n=3	n=4	n=5
BC penalty -- taken	6.0	5.0	4.0	4.0	4.0	4.0
-- not taken	5.0	4.0	3.0	2.0	1.0	0.0

Delayed Branch

The *n* instruction(s) following the branch are executed unconditionally prior to the execution of the branch.

The branch "slots" are filled with useful (nonbranching) instructions by the compiler, or none if there are none.

		n=0	n=1	n=2	n=3	n=4	n=5
Delay BR		4.0	3.0	2.0	1.0	0.0	0.0
Delay BC	-- taken	6.0	5.0	4.0	3.0	2.0	1.0
	-- not taken	5.0	4.0	3.0	2.0	1.0	0.0