Review of R2000-like Pipeline

Though somewhat styleized, the pipeline covered in CSE378 is a realistic example of an implementation for the MIPS R2000 ISA under suitable technological assumptions.

Reviewing the basics of that pipeline is goal of this lecture.

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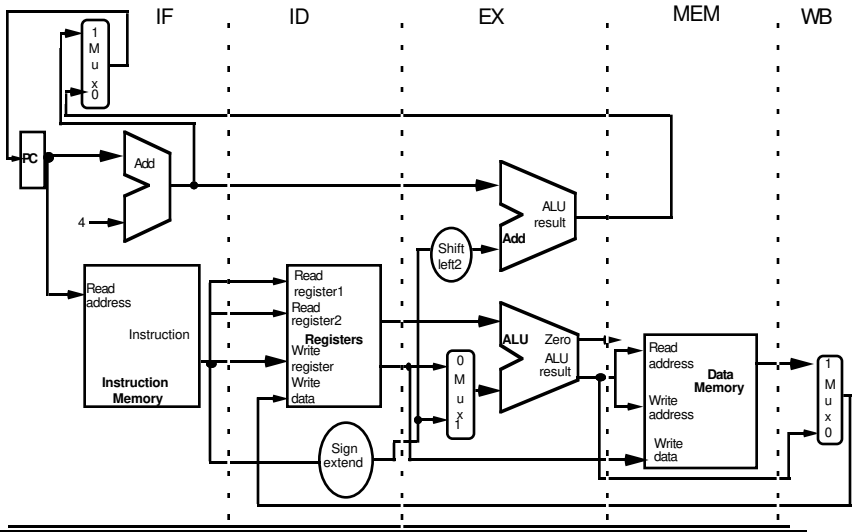
Basic Functional Components, Partitioned



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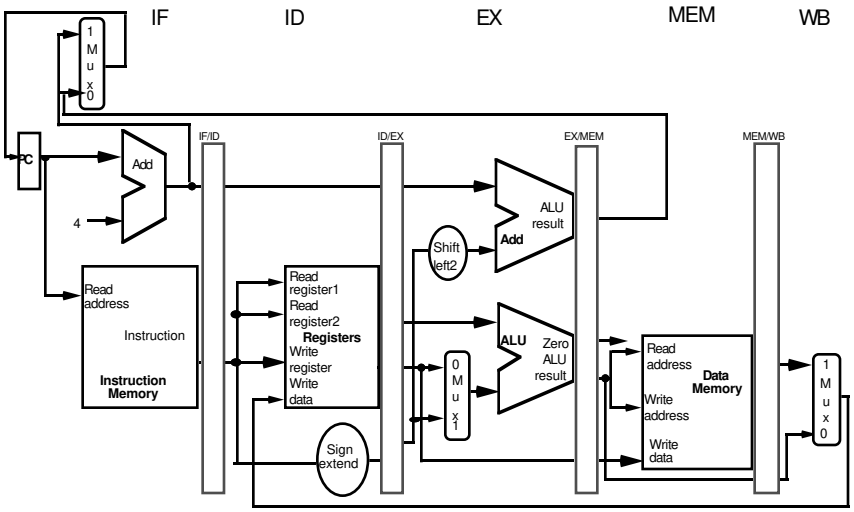
Pipeline Registers



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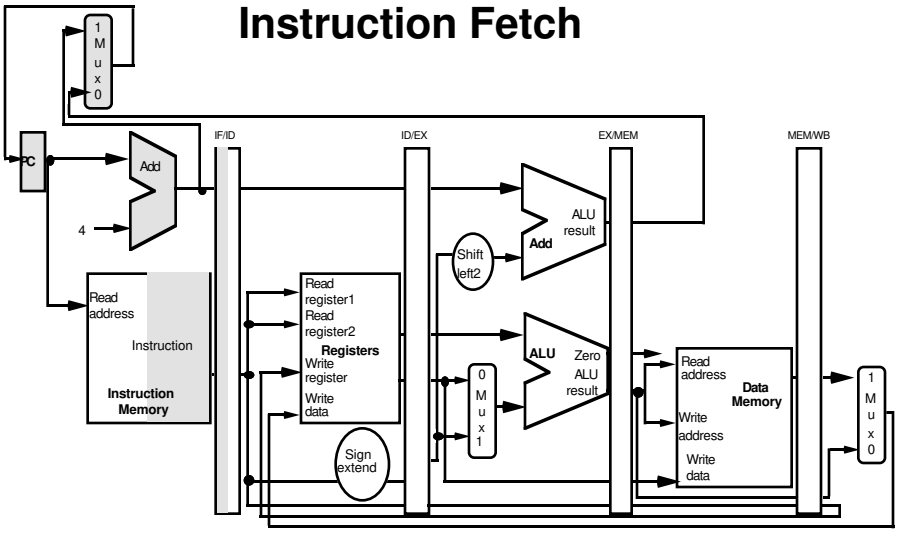
Instruction Fetch



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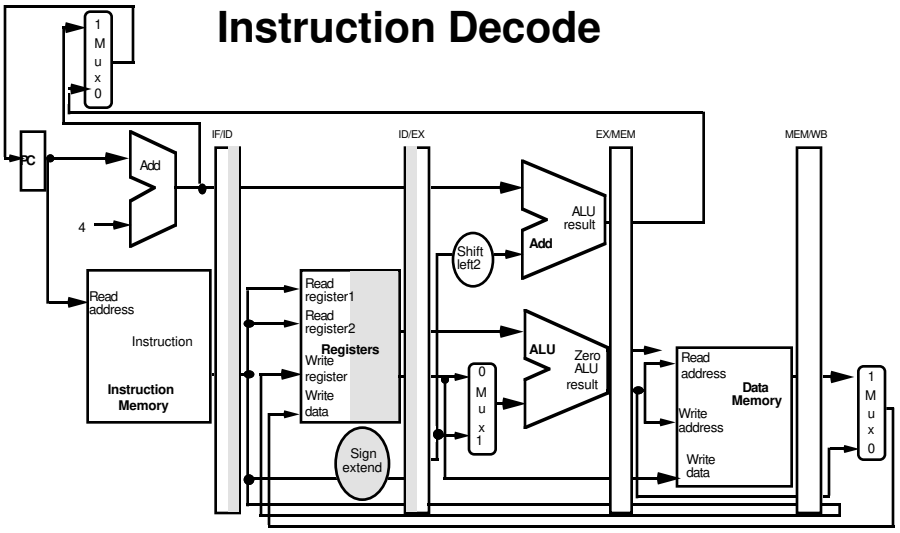
Instruction Decode



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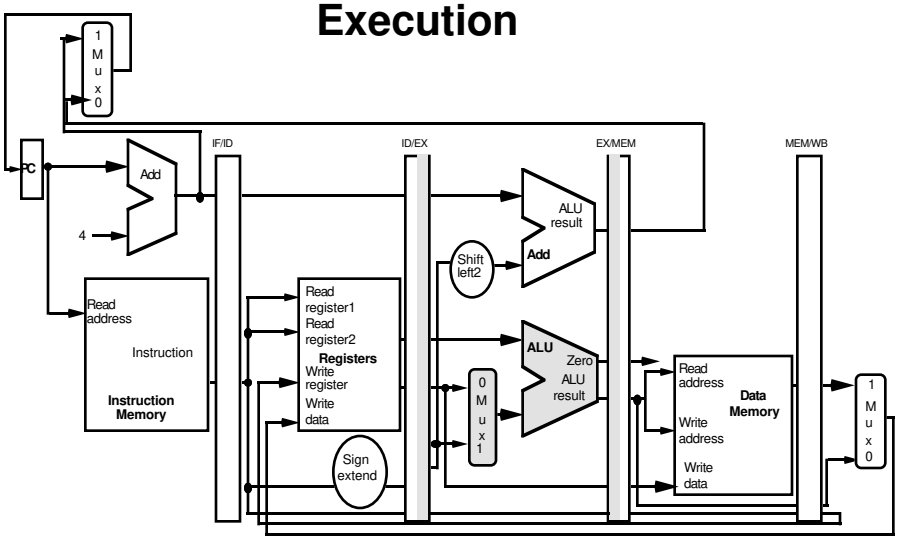
Execution



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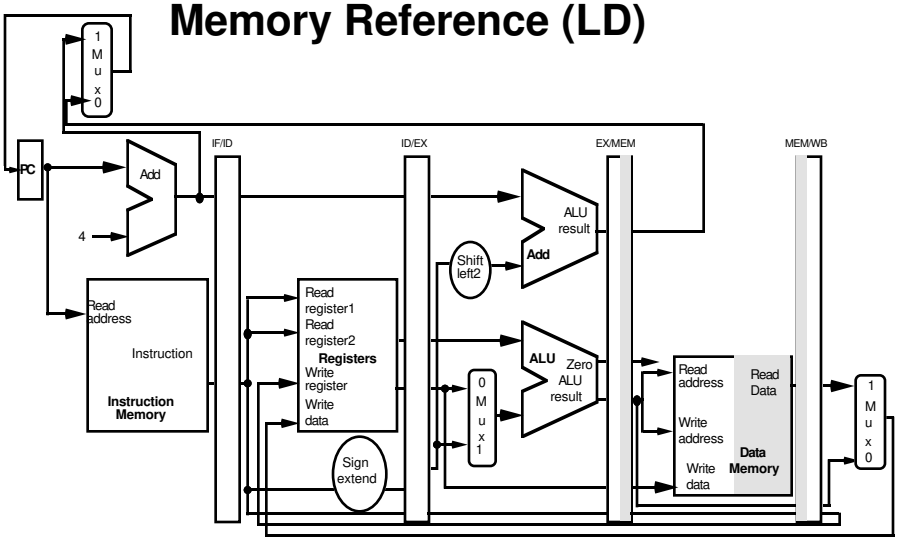
Memory Reference (LD)



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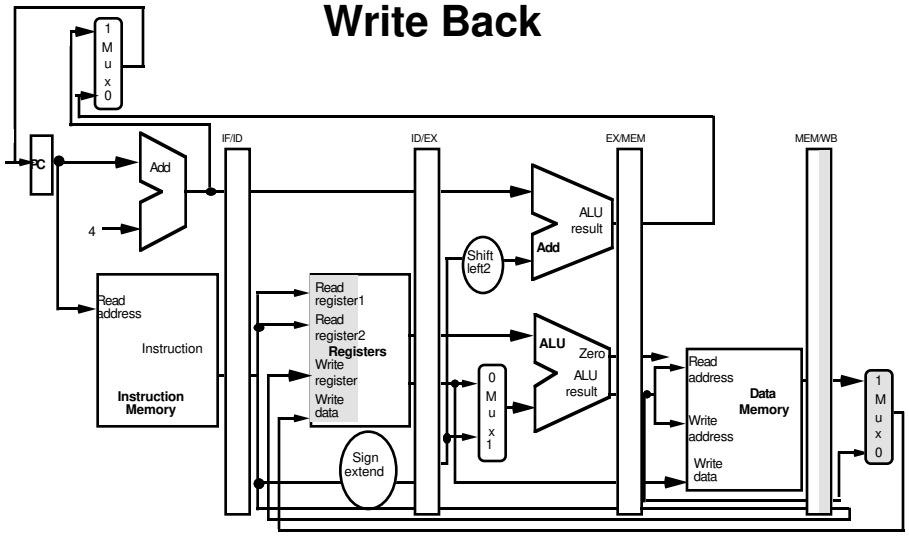
Write Back



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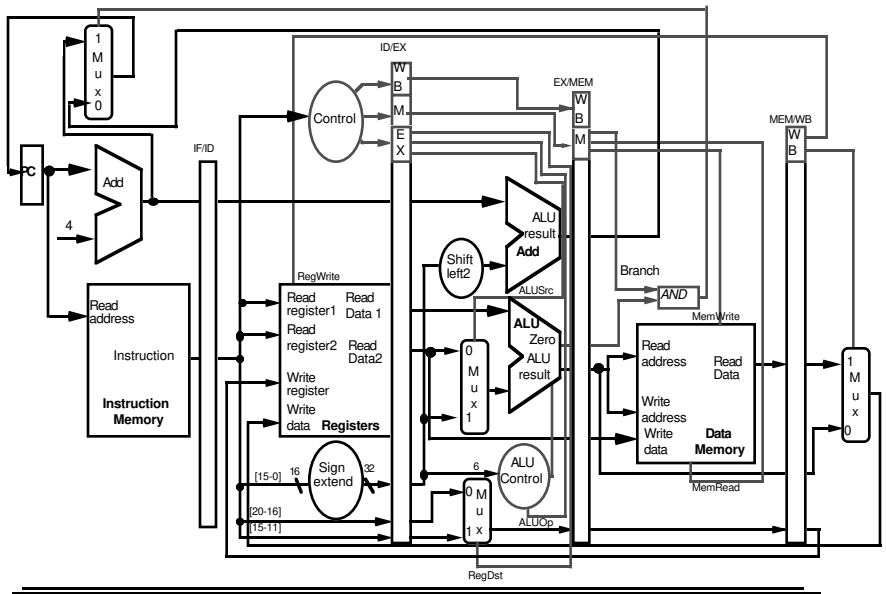
Pipeline Control



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