Assignment 4
Branch Target Buffer

Goal: Design a branch target buffer with 2 bit predictive capability in Verilog and demonstrate that it works. Appreciate the complications of hardware support for Least-recently-used replacement policies.

The BTB will have 64 entries with the following structure:

Branch Instr Addr	Branch Pred Stats	BranchTarget	LRU Data

where

Branch Instruction Address is a 32-bit virtual address (tag),
Branch Target is a 32-bit instruction,
Branch Prediction Statistics is a 2-bit saturating counter that counts up, when the target is selected, and counts down when the in-line alternative is selected.
LRU Data is a 10 bit field used to manage the BTB.

There will be a global counter called LRU time.

Inputs to the BTB are as follows:

Operation -- defined below.
Instruction Virtual Address IVA (32 bits).
Target Instruction (32 bits)

Outputs of the BTB are as follows:

BTB Hit {0 = miss, 1 = hit}
BTB Guess {0 = inline, 1 target}
Instruction (32 bits)

Operation: In selecting an encoding of these values, give some thought to efficiently presenting the information to the BTB to make its circuit design simpler.

Clear -- sets all bits in the Branch Instruction Address field and the LRU Data field to 0; initializes LRU time to 1.

Lookup -- using the address of the IVA input performs an associative search of the BTB on the Branch Instruction Address tag. If no match is found, return BTB Hit = 0; otherwise return BTB Hit = 1, return the msb of the Branch Prediction Statistics field as the BTB Guess, return the contents of the Branch Target field as an output for the Instruction bits, assigns LRU time to LRU Data and increments LRU time.

Verify In-Line -- Locate the branch in the table using the IVA bits, and if found decrement the Branch Prediction Statistics field. Set BTB Hit.

Verify Target -- Locate the branch in the table using the IVA bits, and if found increment the Branch Prediction Statistics field and store the Target Instruction input bits into the Branch Target field. Set BTB Hit.

Insert In-Line -- Find an entry with the smallest LRU Data field, replace its Branch Instruction Address field with the IVA bits, set its LRU Data field to LRU time and increment LRU time, and set its Branch Prediction Statistics field to 1.

Insert Target -- Find an entry with the smallest LRU Data field, replace its Branch Instruction Address field with the IVA bits, replace the Branch Target field with the Branch Target bits, set its LRU Data field to LRU time and increment LRU time, and set its Branch Prediction Statistics field to 2.

Task: Create a behavioral Verilog design of the BTB and demonstrate its correct operation.

Answer for your design the following questions:

1) What is the rationale behind the encoding you chose for the operation field?
2) As specified, the LRU field simply counts up continuously. This strategy has some potential difficulties, such as the fact that it could eventually overflow. This will cause a branch to be entered into the table at a low LRU Data value, which will make it a victim on the next entry, etc. How might this problem be fixed? Justify that your solution is efficient.

Turn in: The design, the evidence of its correct operation, and the answers to the questions are due Monday 18 November 1996 at 5:00 P.M.