# Architectural Implications of Brick and Mortar Silicon Manufacturing

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### Cost of Production

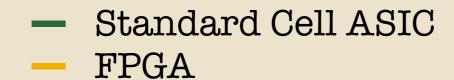
- Standard Cell ASIC

**Production Cost** 

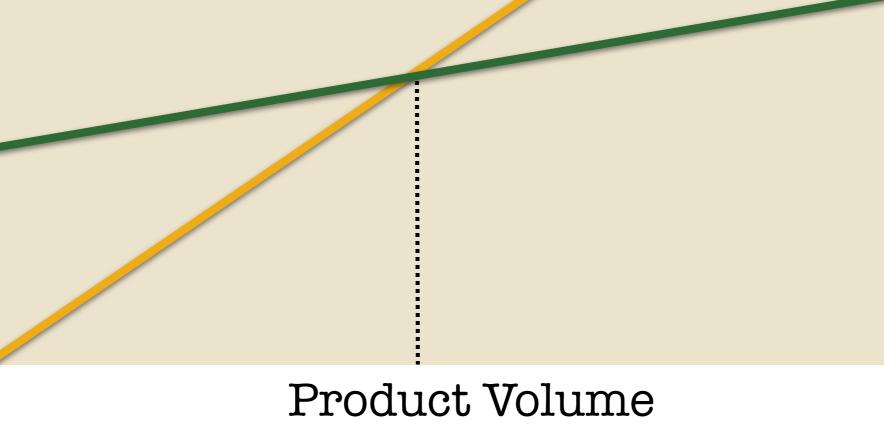


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## Cost of Production



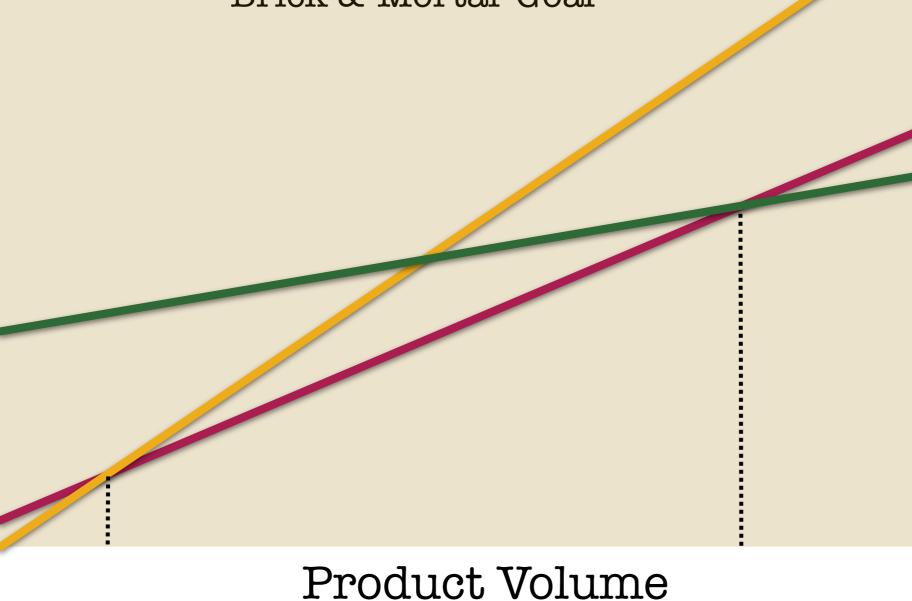
**Production Cost** 



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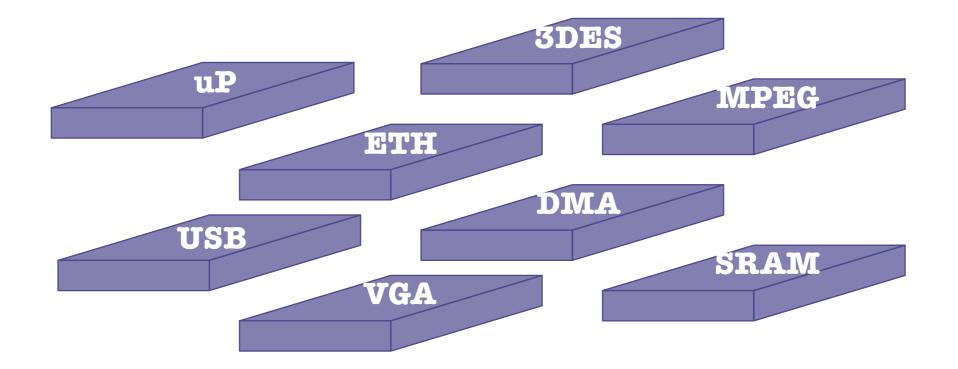
## Cost of Production

- Standard Cell ASIC
- FPGA
- Brick & Mortar Goal



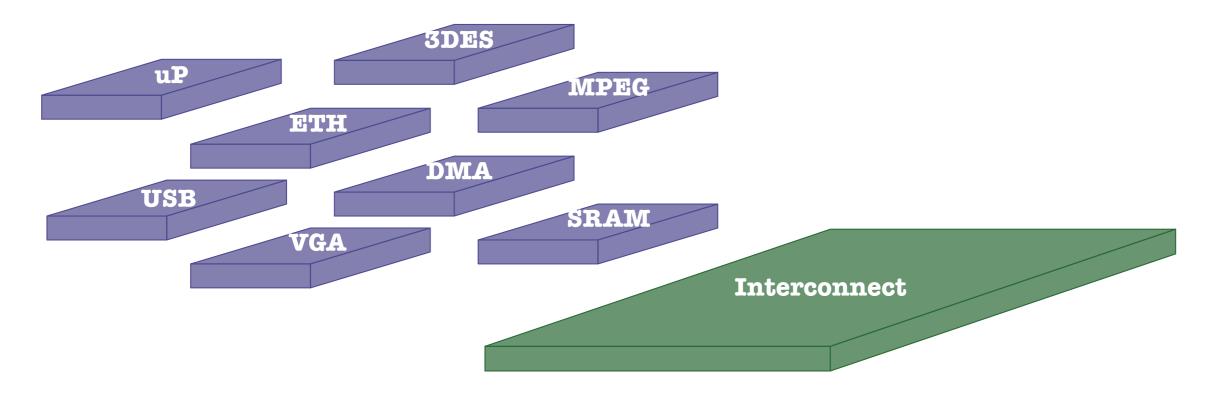
#### 1. Bricks

- Mass-produced ASICs
- Standard interface
- Fixed set of functions



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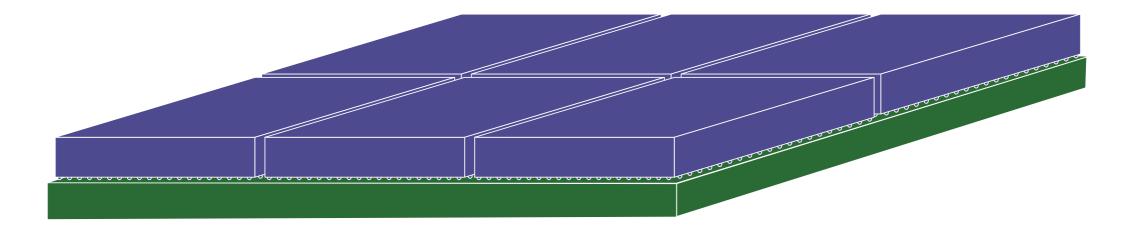
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- 2. "Mortar"
  - Mass-produced ASIC
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- 3. Assembly
  - Alignment
    - e.g. robotics, fluidic
  - Bonding
    - e.g. flip-chip, proximity

### Benefits of Brick and Mortar

- **Chip manufacture**: mask-free, fab-free, improved yields
- Chip performance: mostly ASIC
- Chip design: uses today's SoC design flow

## Why Should Architects Care?

- Good architecture essential for viability
  - Brick function and form-factor
  - Inter-brick interconnect design

## Outline

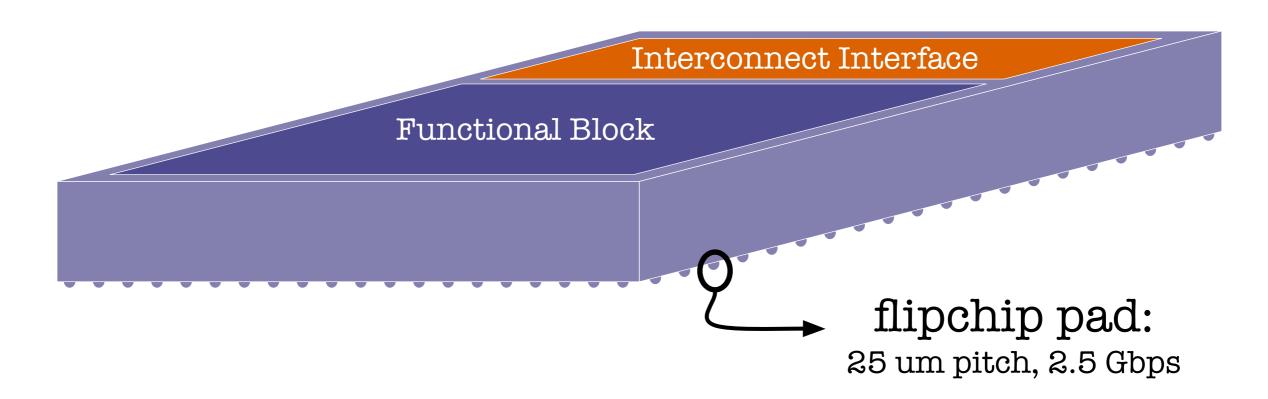
#### • Brick and Mortar Chips

- Definition
- Potential
- Architectural Questions
- Brick and Mortar Architecture
  - Bricks
  - Interconnect

#### • Brick and Mortar Assembly

- Options
- Interaction with architecture

### Brick Form Factor

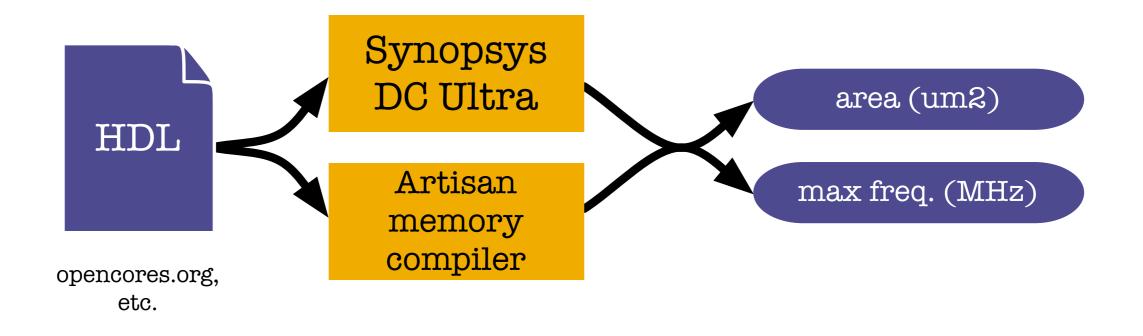


• Each brick . . .

#### • is square

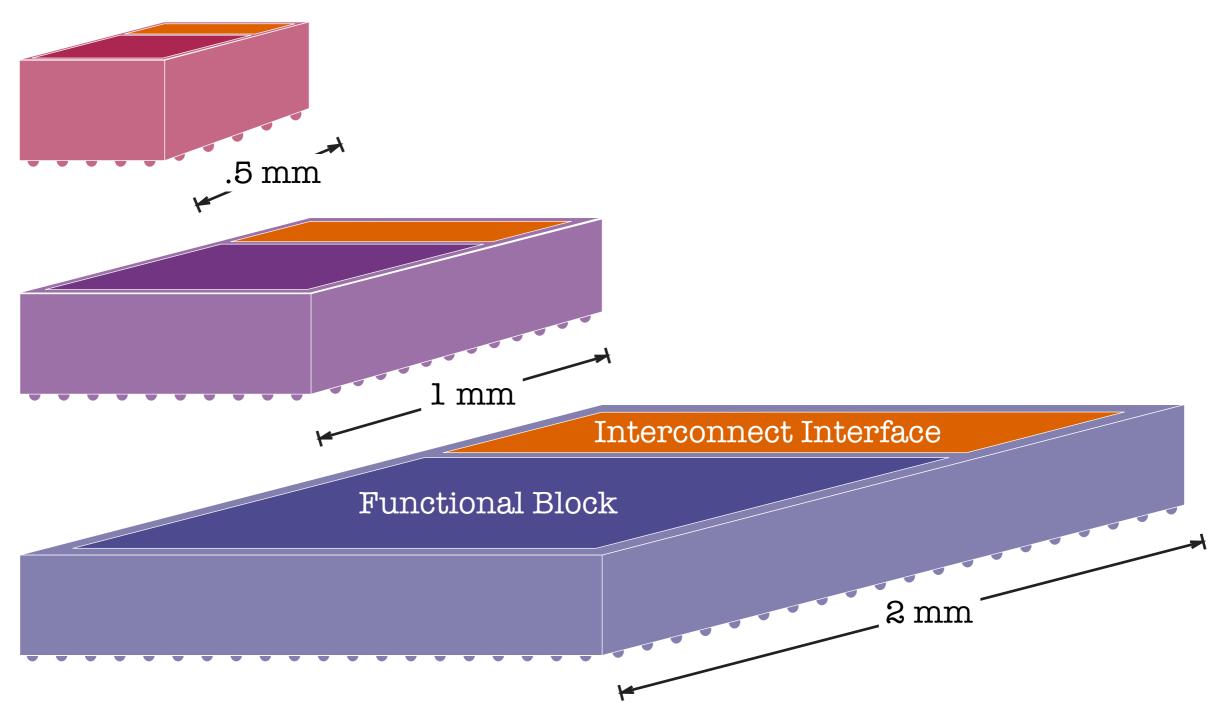
- has 15% of area reserved for extra circuitry
- has one surface covered with flipchip pads

### Brick Architecture



Function Description	Area (um2)	Max Freq. (MHz)
USB 1.1 Physical Layer	2,201	2941
JPEG Decoder	625,457	629
RISC Core + 256K Cache	3,111,025	1087

### Multiple Brick Sizes



## Brick Size Selection

Function	Cir	cuit	Freq. R	ange at Brick	Size
Description	Area (um2)	Max Freq. (MHz)	Small	Medium	Large
256 K SRAM (single-ported)	2,729,344	2315	No Space	No Space	N/A - 2315
JPEG Decoder	625,457	629	No Space	N/A - 629	No Benefit
VGA/LCD Controller	4,301	1219	N/A - 1046	N/A - 1219	No Benefit

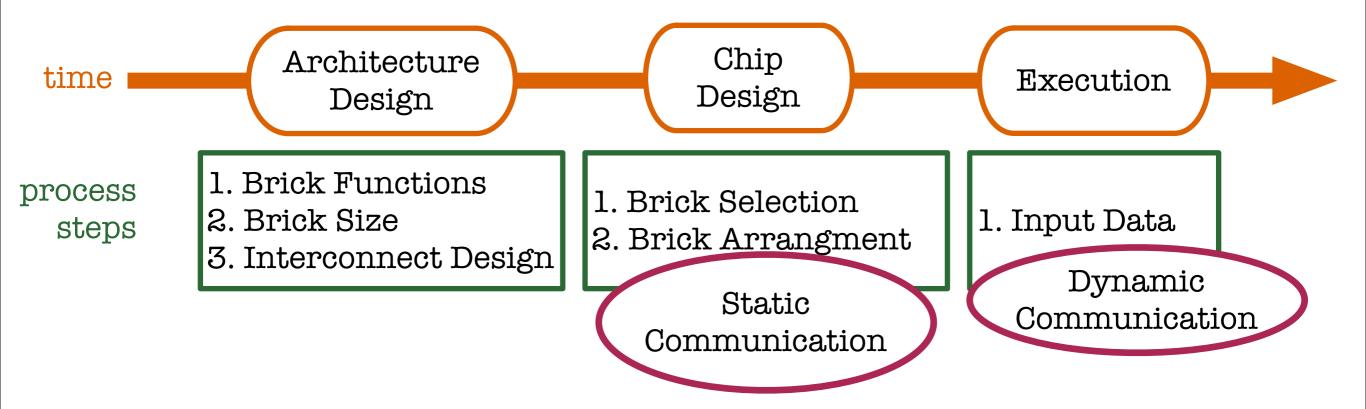
• Smallest brick to fit circuit, unless bandwidth **severely** constrained

## Outline

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- Definition
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  - Bricks
  - Interconnect
- Brick and Mortar Assembly
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### Interconnect Dilemma



- General purpose interconnect facilities
  - Communication known at design time  $\rightarrow$  configurable wires
  - Dynamic communication

 $\rightarrow$  packet-switched net

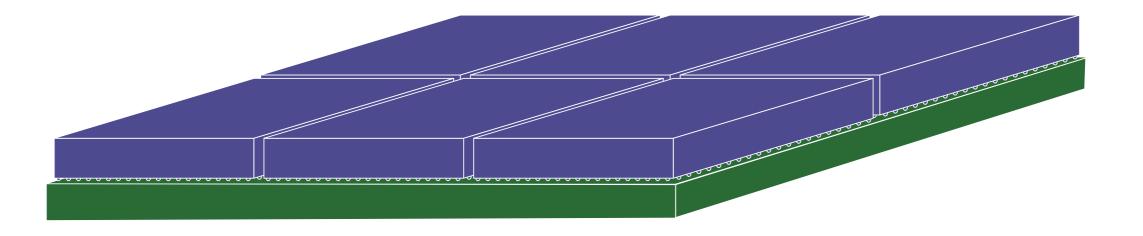
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#### • Alignment

- Robotic
- Self-Assembly
- Martha + tweezers
- ...

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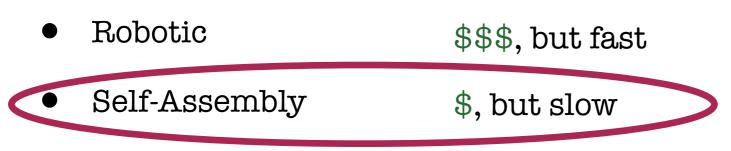
- Robotic \$\$\$, but fast Self-Assembly \$, but slow
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  - ...

#### Bonding

- Flip-chip medium-density, but more robust connection
- Proximity

- high-density

#### • Alignment



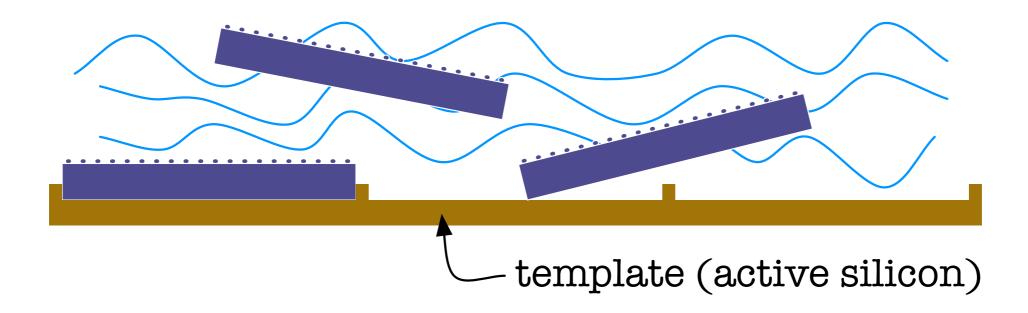
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• Flip-chip	medium-density, but more robust connection
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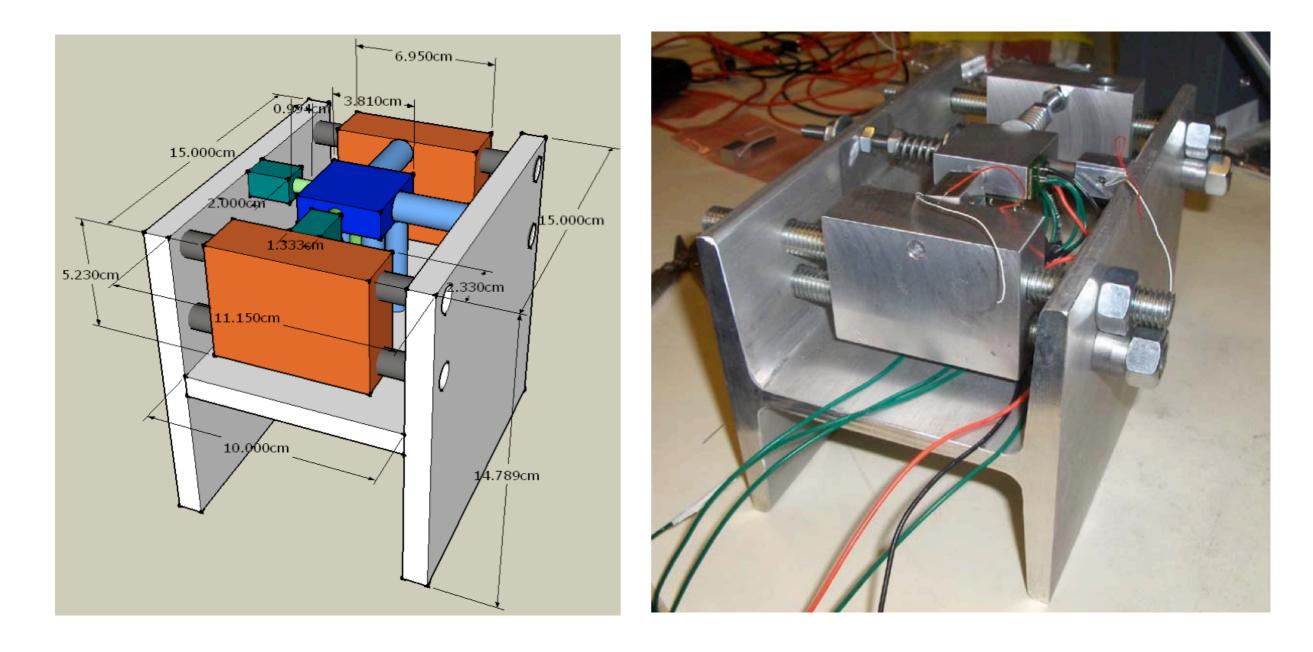
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### Alignment: Fluidic Self Assembly



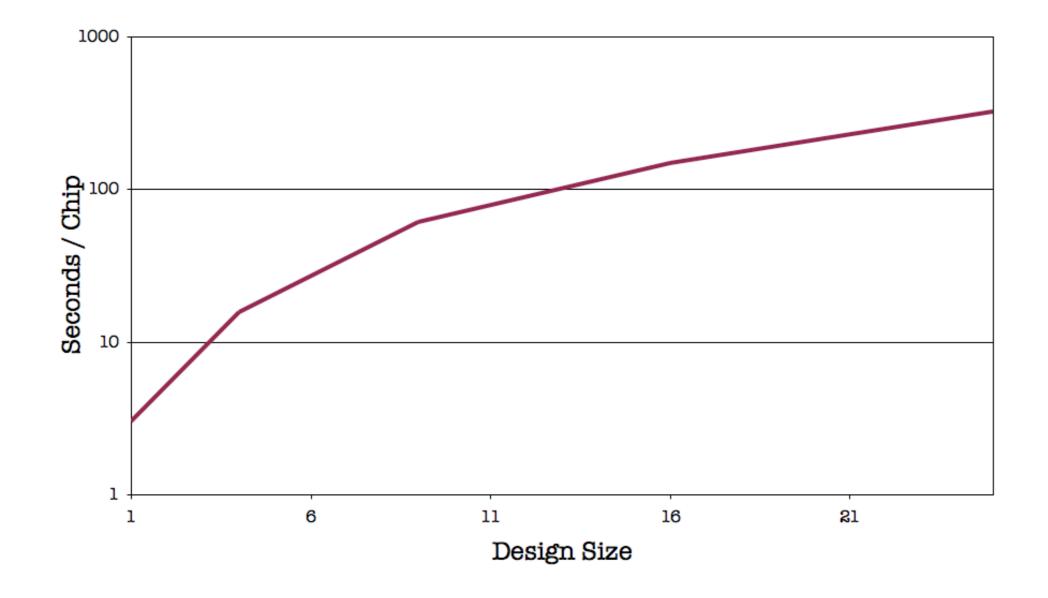
- Template brick communication via proximity communication
  - Brick type check, BIST, speed grade
- Polymer on template can grip or eject bricks

### Alignment: Fluidic Self Assembly



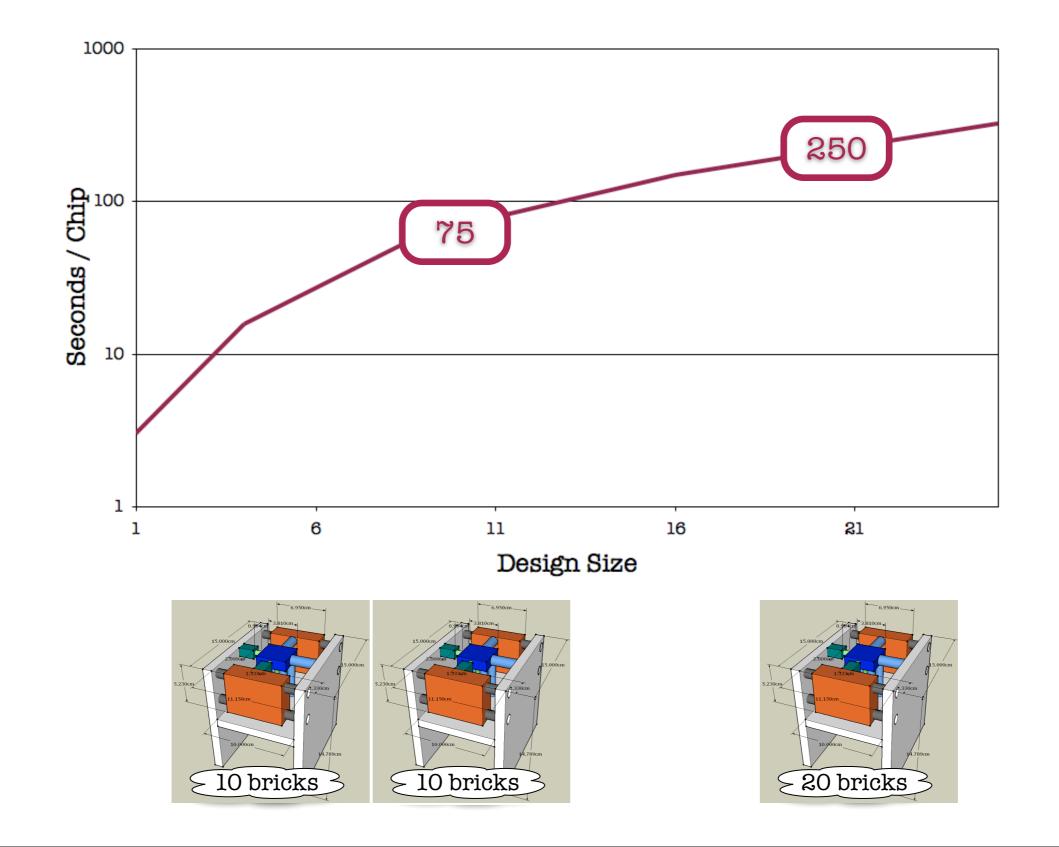
• Washington EE experimental system

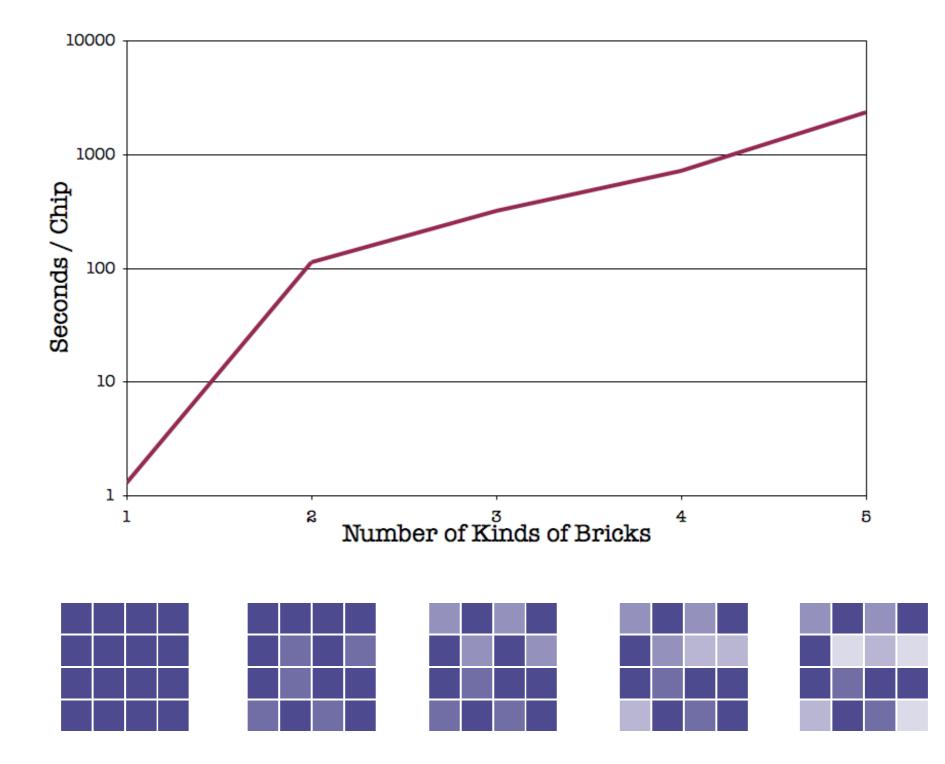
### Assembly Time v. Number of Bricks

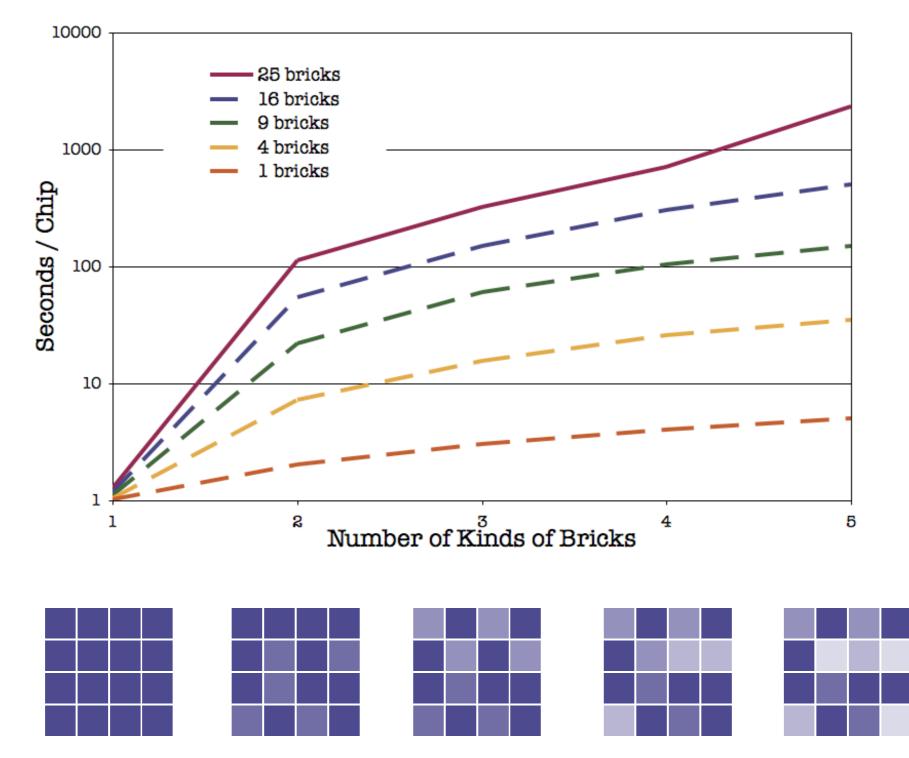


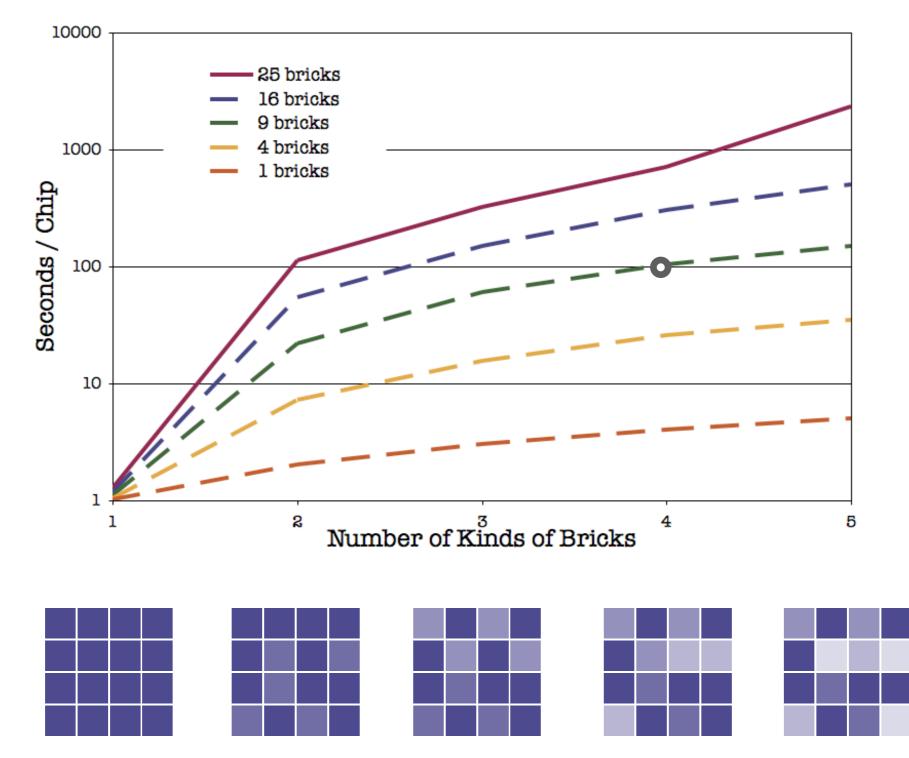
• Statistical simulator driven by experimentally derived rates of assembly and disassembly

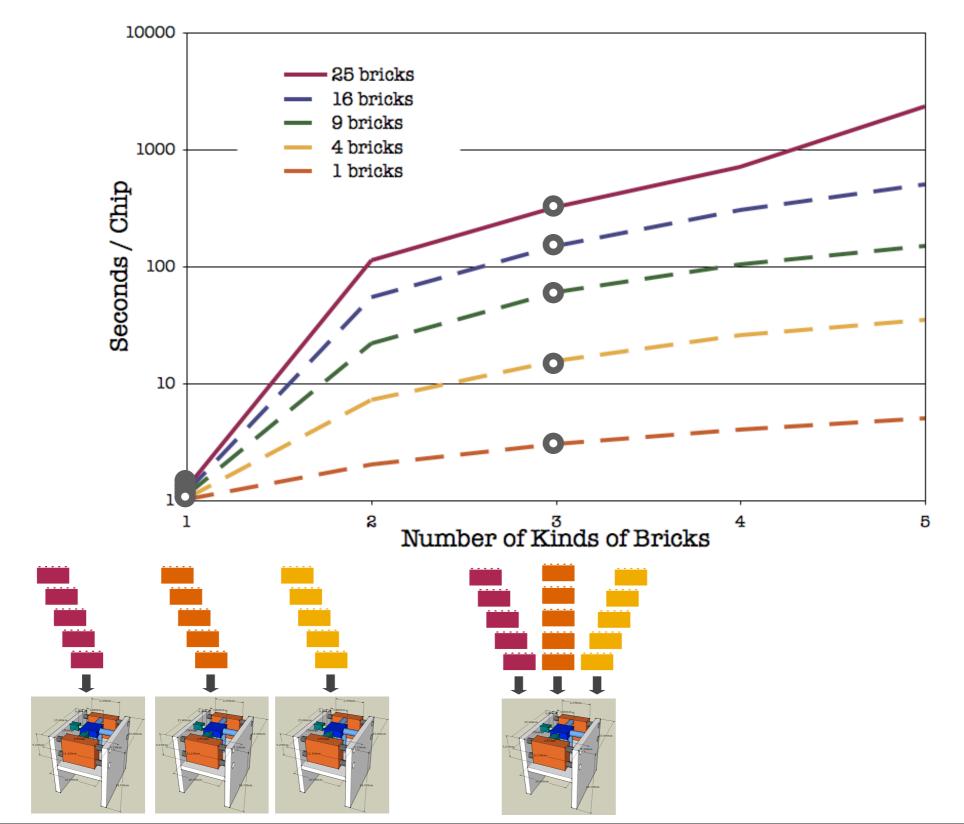
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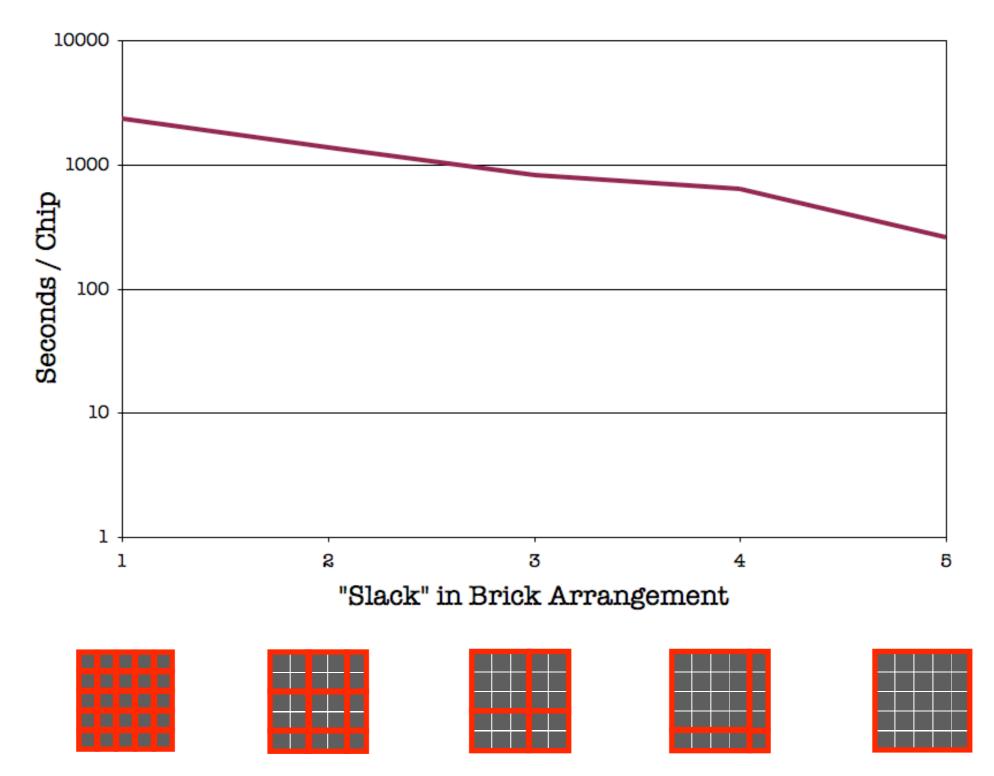




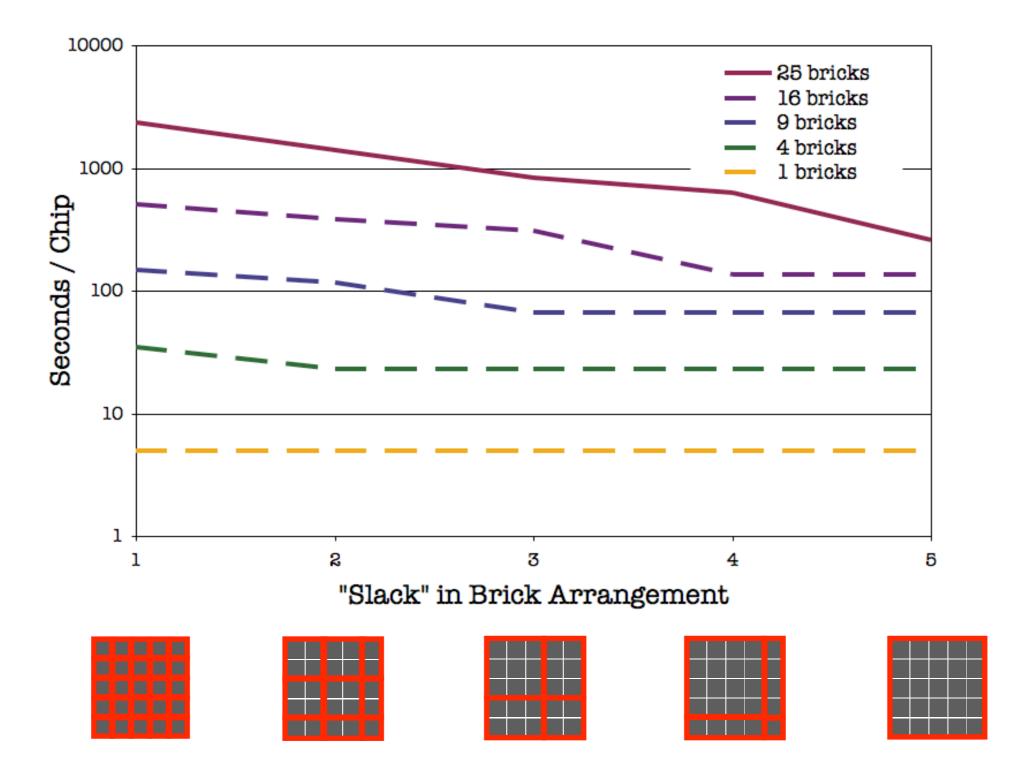




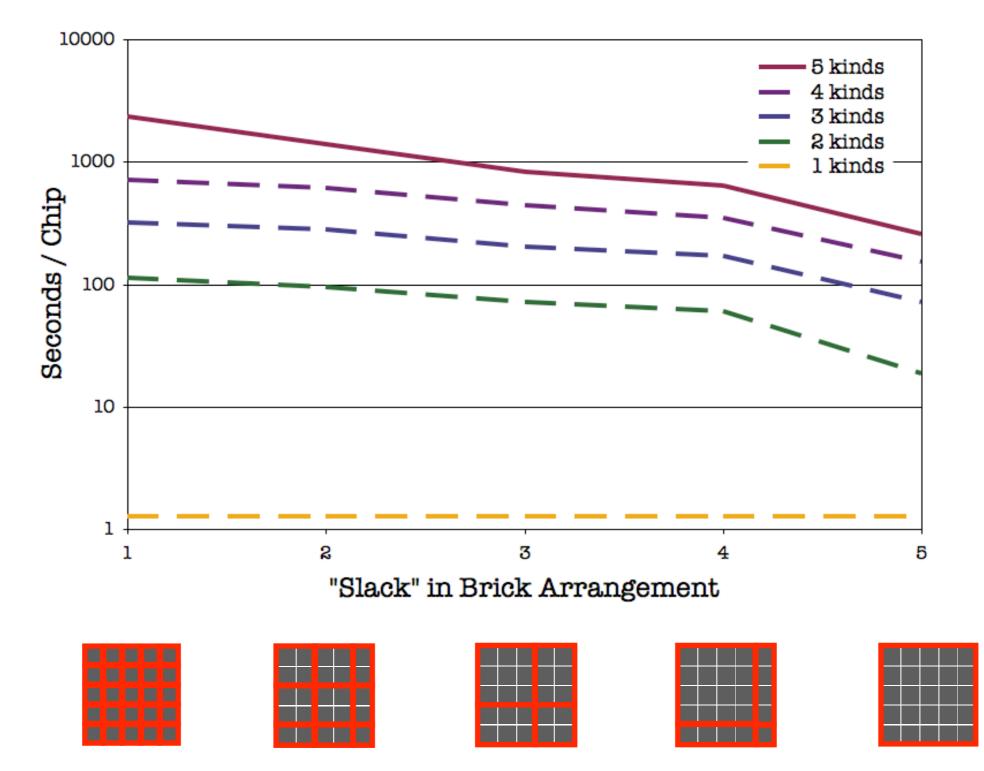
### Assembly Time v. Brick Arrangement Slack



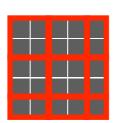
### Evaluating Slack: Design Size

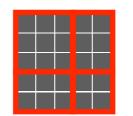


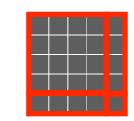
### Evaluating Slack: Brick Kinds

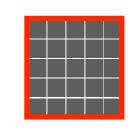


### Evaluating Slack: Brick Kinds









### Assembly and Architecture

#### • Architecture can assist assembly by

- Reducing the number of kinds of bricks
  - i.e., two brick kinds v. one slightly reconfigurable circuit
- Accommodating variable assemblies

### Conclusion

Brick and Mortar process offers ASIC-like chips without the masks and fabs

Architecture is crucial to meet the performance goals of the process

With low-cost assembly techniques, can meet the economic goal as well