Computer Design and Organization

Assignment #6

Due: Wednesday December 12

The purpose of this last assignment is to sharpen your understanding of snoopy cache coherence protocols. Once again, you can do this homework by yourself or with a partner with whom you have not worked with before.

1. Problem 8.4. (this should not be too difficult since a solution is in the slides!). Explain what happens on the sequence:

	Processor P1	Processor P2	Processor P3
Time 1	Read A	-	-
Time 2	-	Read A	-
Time 3	-	-	Read A
Time 4	Read B	-	-
Time 5	-	Write A	-
Time 6	-	-	Read A
Time 7	-	Read B	-
Time 8	-	-	Read B

   where A and B are two different memory lines mapping to the same cache line (assume that the caches are direct-mapped and therefore a miss to B forces A to be replaced).

   Of particular interest are your choices for:

   - Who produces the value of A at time 2 for P2?
   - When is the dirty value of A written back to memory? (Note the same value can be written back more than once but not necessarily in this example.)

2. Problem 8.5