Computer Design and Organization
Outline (subject to change)

1. Introduction and goals.
2. The MIPS 2000/3000 pipeline (review – From H&P)
3. Introduction to Verilog (see on-line manual)
4. Branch prediction (see hand-out)
5. Processors with multiple pipes
6. Superscalar processors (Sohi and Smith survey)
7. Out-of-order processors
8. VLIW – EPIC ISA's
9. Caches (review – From H&P)
10. More on caches (see hand-out)
11. Main memory (Synchronous DRAMs; Rambus)
12. Symmetric multiprocessors. Cache coherence (Archibald and Baer paper)
13. Synchronization (see hand-out)