CSE 471 Winter 2000

# Computer Design and Organization

**Where and When**
Lectures: EEB 108 MWF 10:30-11:20

**Instructor**
Jean-Loup Baer, 211 Sieg Hall, 685-1376, baer@cs
Office hours: M 2:30-3:30 F 1:30-2:30 or by appointment.

**Teaching Assistants**
Vivek Sahasranaman (svivek@cs) Office hours: TBA
Tim James (tjames@cs) (half-time) Office hours: TBA

**Course Goals and Material to be covered**
The first part of the course will be devoted to the thorough understanding of the design and implementation (at the register transfer level) of pipelined processors. We'll start with a review of the pipelines of first generation RISC microprocessors (this will be the basis for the course project, an implementation and extension in Verilog of the MIPS R2000/3000 pipeline). We'll then look at hardware assists such as Branch Predictors and at more complex pipelines like those found in superscalar processors and dynamically scheduled processors. In the second part of the course, we'll study some modern enhancements of cache memories. Finally, we'll touch on some (hardware) issues for symmetric multiprocessors.

Knowledge of the material taught in CSE 370 and CSE 378 is assumed.

**Text:**
D.Patterson and J.Hennessy *Computer Organization & Design: The Hardware/Software Interface* 2nd Edition, 1998

Additional survey papers from the literature will be distributed.

On-line Verilog manuals and tutorials.

**Assignments:**
All assignments will be Verilog programs. The goal of the first two or three assignments will be to review the basic pipeline structure and to familiarize yourselves with Verilog. The next one or two assignments will be to design – and test – some hardware assists. The project, to be done in groups of two, will be the design, Verilog implementation and testing of the MIPS 2000/3000 pipeline to whcih we'll attach some fo the assists you'll have designed (we won't simulate the complete instruction set!).

Please hand in your assignments, electronically, on the due date. Late assignments will not be accepted.

**Exams**:
Alas, there will be some: 1 midterm and 1 final.

**Grading:**
Assignments before project 20%; project 40%; midterm 15%; final 25%. These percentages are approximate. Intangibles may arise. Class participation is a bonus. (Class participation is strongly encouraged. Don't be afraid to ask questions: by definition, there are no dumb questions. If I ask you a question and you don't know, just say so. That's no problem. I will certainly answer some of your questions also by "I don't know!".)

**e-mail and WWW**
We will have a class mailing list and we will communicate often through e-mail. Feel free to send the TA's or me questions. We will forward questions and answers to the whole class if appropriate. Check the CSE471 home page frequently.