CSE 469

Winter 2019

ABOUT ME: MARK OSKIN

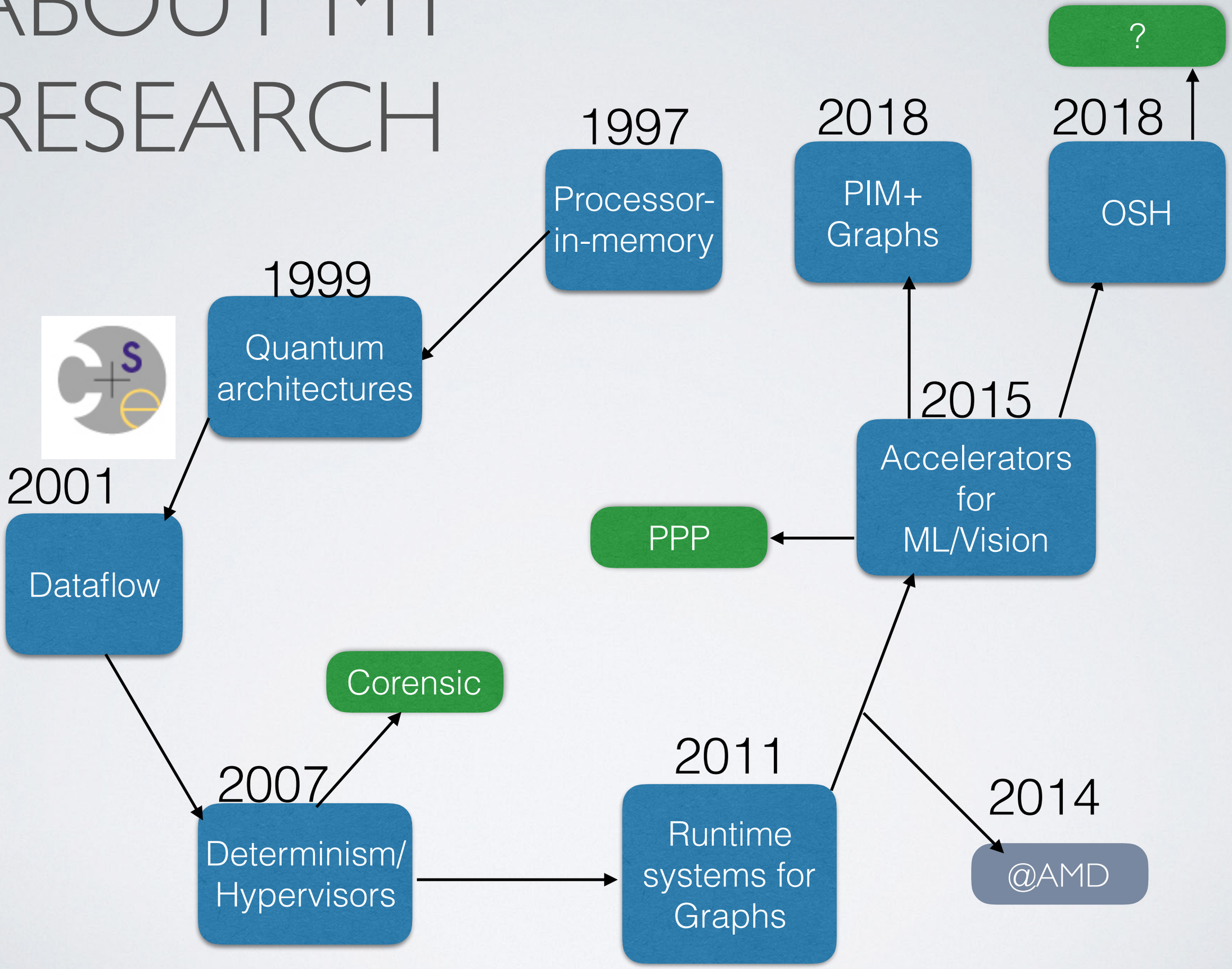
I don't do email, but I do respond to txt messages: 206-293-9456

OH: Wednesday 9:30 - 10:30, CSE 480, but happy to SkyPE / ZOOOM by appointment.

Writing software & designing hardware for 37 years. I hate computers & technology.

I'm a morning person and go to bed at 7pm. I live in two worlds (Whidbey & Edmonds).

ABOUT MY RESEARCH

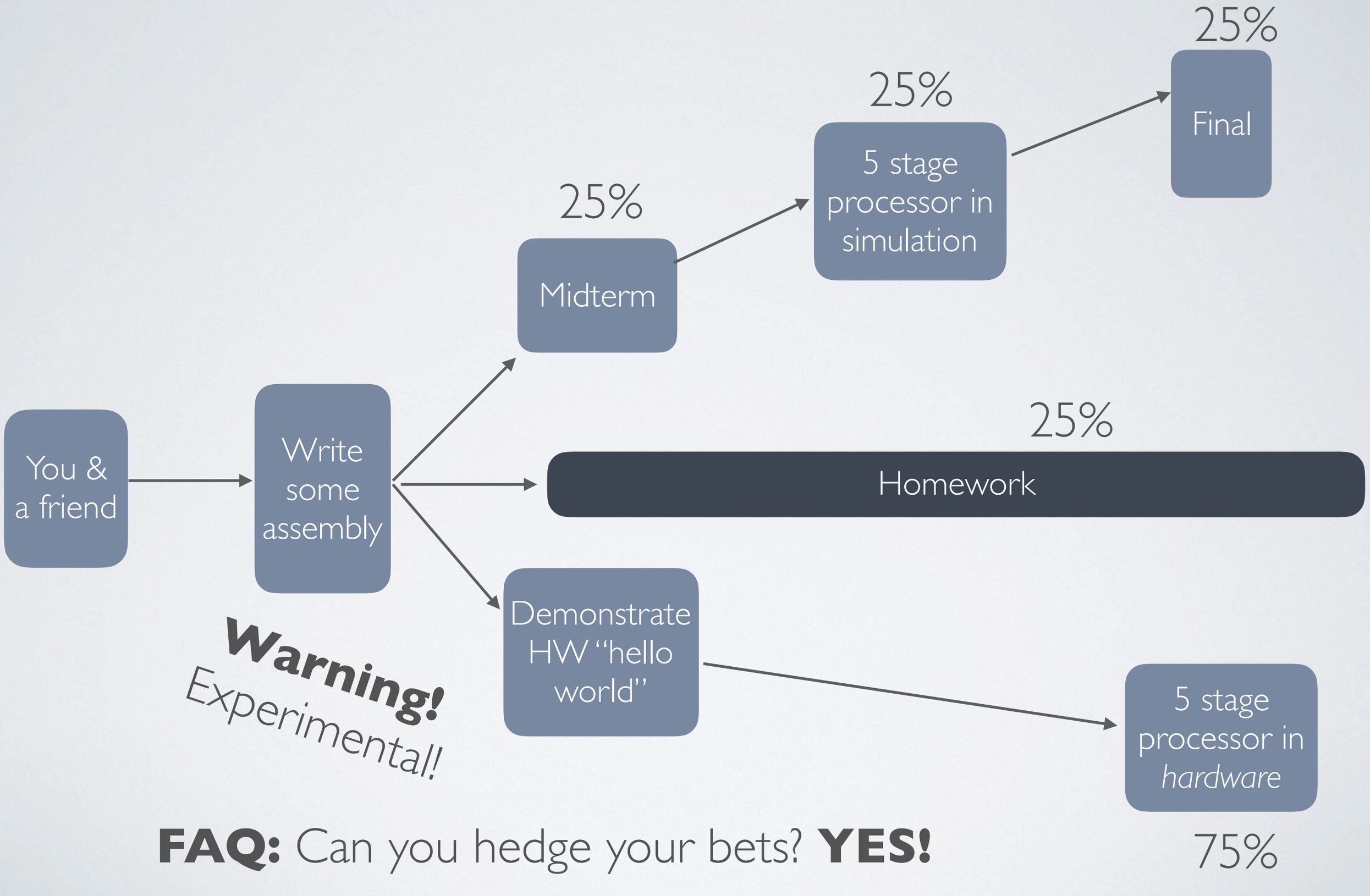


WHO ARE YOU?

WHAT IS 469

- How computers actually work
- Assembly programming (2 weeks)
- "Canonical" 5 stage pipelined processor (4 weeks)
- How to make processors fast(er) (2 weeks)
- A glimpse beyond the CPU (1 week)

TWO PATHS TO 469 SUCCESS



FAQ: Can you hedge your bets? **YES!**

THE HARDWARE PATH

TinyFPGA BX

If you choose this path you & your friend need to supply your own hardware. Unfortunately CSE/ECE does not have the support infrastructure anymore to loan it to you.

Downside: it costs $40. Upside: you get to keep it.

If you really want to do the hardware path and $40 is the issue, contact me privately and I'll take care of it.

You can buy these from Amazon, tindie, digikey, and from tinyfpga directly.

FAQ: Can I use my own hardware if I already have it? **YES!**
But we can't necessarily support you as well. YMMV.

HW PATH (CONTINUED)

- TinyFPGA BX contains the ICE40LP8K chip.
  - Has a complete open source tool chain, which is what we will be using.
    - FAQ: Yes the toolchain is ….buggy… they all are.
    - FAQ: Yes you can use the commercial tool chain if you want. It's free.
- Has support for about 7000 gates. Of these, about 1500-3000 will be used by the "debugger".
- 4000-5000 gates is not a lot. Because of this the HW path will implement a stripped down **32 bit *(most likely)*** ARM processor. Software path **64 bit**.

THE "SOFTWARE" PATH

- Design canonical 5 stage pipelined processor in Verilog.
- But only has to work correctly on iverilog or verilator.
  - Don't underestimate the leap from simulation only based design to real HW. The gap is in discipline, feedback and time (frustration).

BY WEDNESDAY

- **Choose a partner.** Yes you can do the homework and project alone, but it is not recommended.

- **Choose a path.** If you are choosing the HW path, buy the HW ASAP.

HOW TO FAIL THIS CLASS

- Don't do the project or start the project too late. **The project is hard.**
- Don't show up to class, particularly if you want to pass the midterm and final.
- Don't produce working homework or project solutions. You can test your designs to success. **There's no reason to turn in a non working solution.**
- Don't work as a team with your partner. We will interview you separately for each milestone in the project. We do this specifically to identify if one team member is "slacking".

HOW TO SUCCEED

- Start homework and projects early.
- Test your designs carefully.
- Work effectively as a team.
- Start small but sure with your knowledge, and build
- You don't necessarily need to take notes in class or even read the book, but you do need to learn the way that you learn best.
    - e.g. I never read the textbook for a class. But what I discovered is if I showed up to lecture and took notes — even if I never read them, which was often the case — then I did fine.
    - Caveat: I know many of you learn from reading too. The key is to know yourself and do what is best for you.

HOW I VIEW MY JOB FOR YOU

- Lecture:
  - I give you the high level view of whats going on
  - I separate the wheat from the chaff for you
  - In other words, I hope to teach you to fish, not to give you a fish :)
- Outside of lecture:
  - I'll be building this processor too, with you. **Through shared suffering…**
    …hopefully I can help you with details.
- What you won't get from lecture:
  - Precise details. You need to pick these up from the reading materials and from doing the homework/labs.
- **In summary, show up, pay attention and work hard. If you do this and fail, then I failed you. But if you don't do these things and fail, then you failed yourself.**

Kind of a metaphor for life?

OTHER RANDOM THINGS

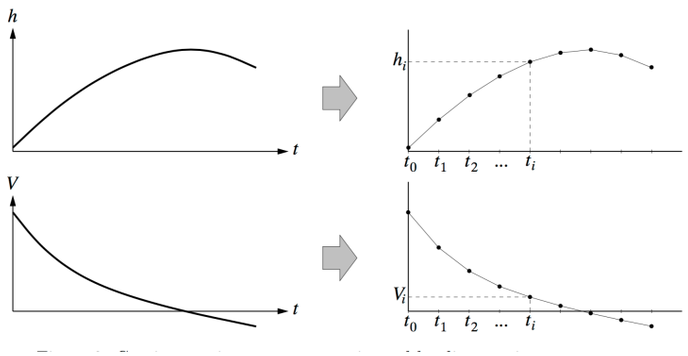
- Lecture is 2 hours long. If I forget, please remind me that we all need to stop and take a break mid way.

- There isn't actually a need for 2 hours of lecture.

    - We'll spend some time doing "office hours" like things and tutorials and such.

http://www.antiquark.com/sliderule/sim/n909es/virtual-n909-es.html

The governing ODEs (5) and (6) can then be used to determine the discrete rates at each



$$\dot{h}_i = V_i \tag{7}$$

$$\dot{V}_i = -g - \frac{1}{2}\rho V_i |V_i| \frac{C_D A}{m} \tag{8}$$

As shown in Figure 3, the rates can also be approximately related to the changes between two successive times.

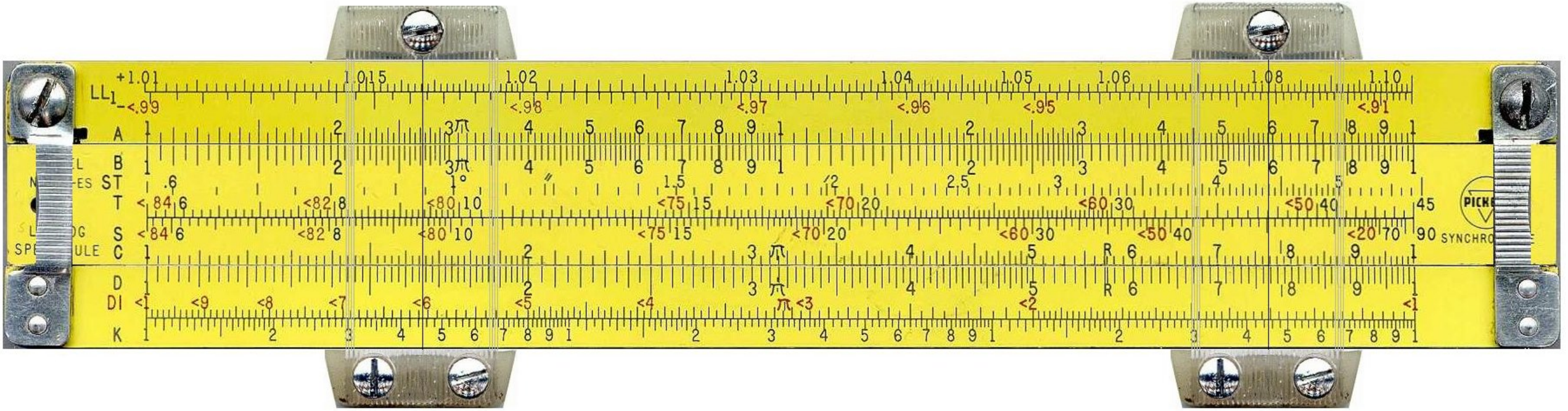
$$\dot{h}_i = \frac{dh}{dt} \simeq \frac{\Delta h}{\Delta t} = \frac{h_{i+1} - h_i}{t_{i+1} - t_i} \tag{9}$$

$$\dot{V}_i = \frac{dV}{dt} \simeq \frac{\Delta V}{\Delta t} = \frac{V_{i+1} - V_i}{t_{i+1} - t_i} \tag{10}$$

Equating (7) with (9), and (8) with (10), gives the following *difference equations* governing the discrete state variables.

$$\frac{h_{i+1} - h_i}{t_{i+1} - t_i} = V_i \tag{11}$$

$$\frac{V_{i+1} - V_i}{t_{i+1} - t_i} = -g - \frac{1}{2}\rho V_i |V_i| \frac{C_D A}{m} \tag{12}$$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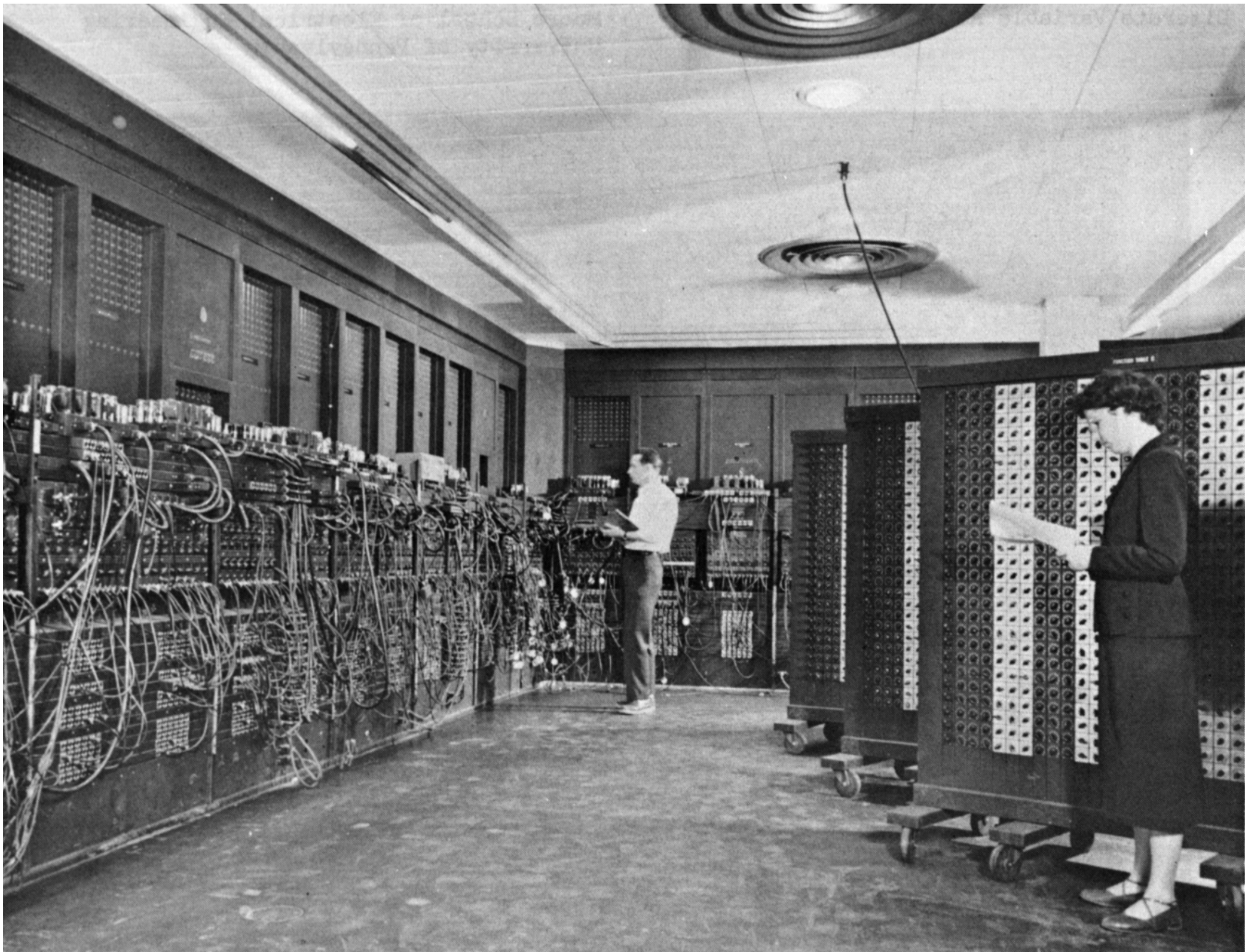
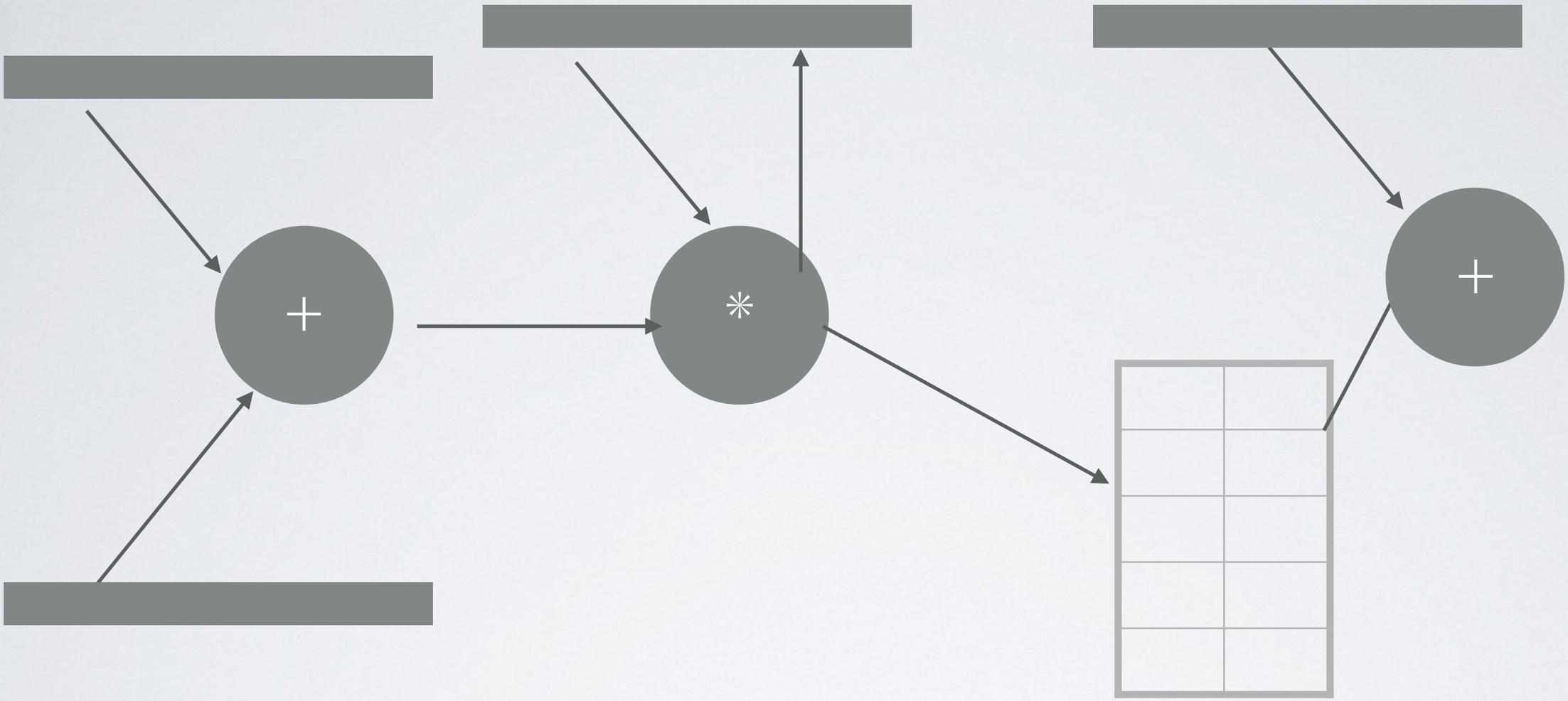
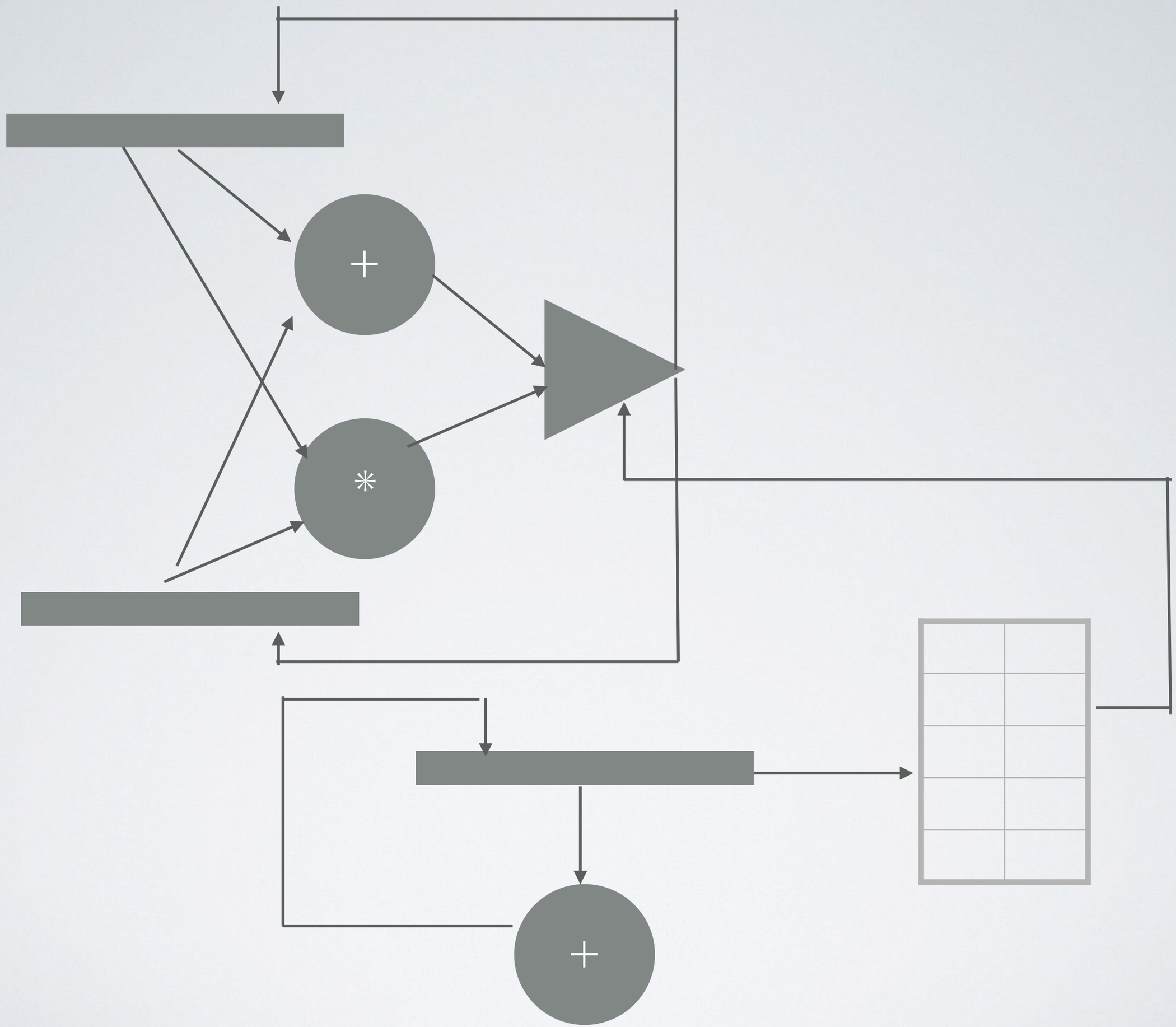
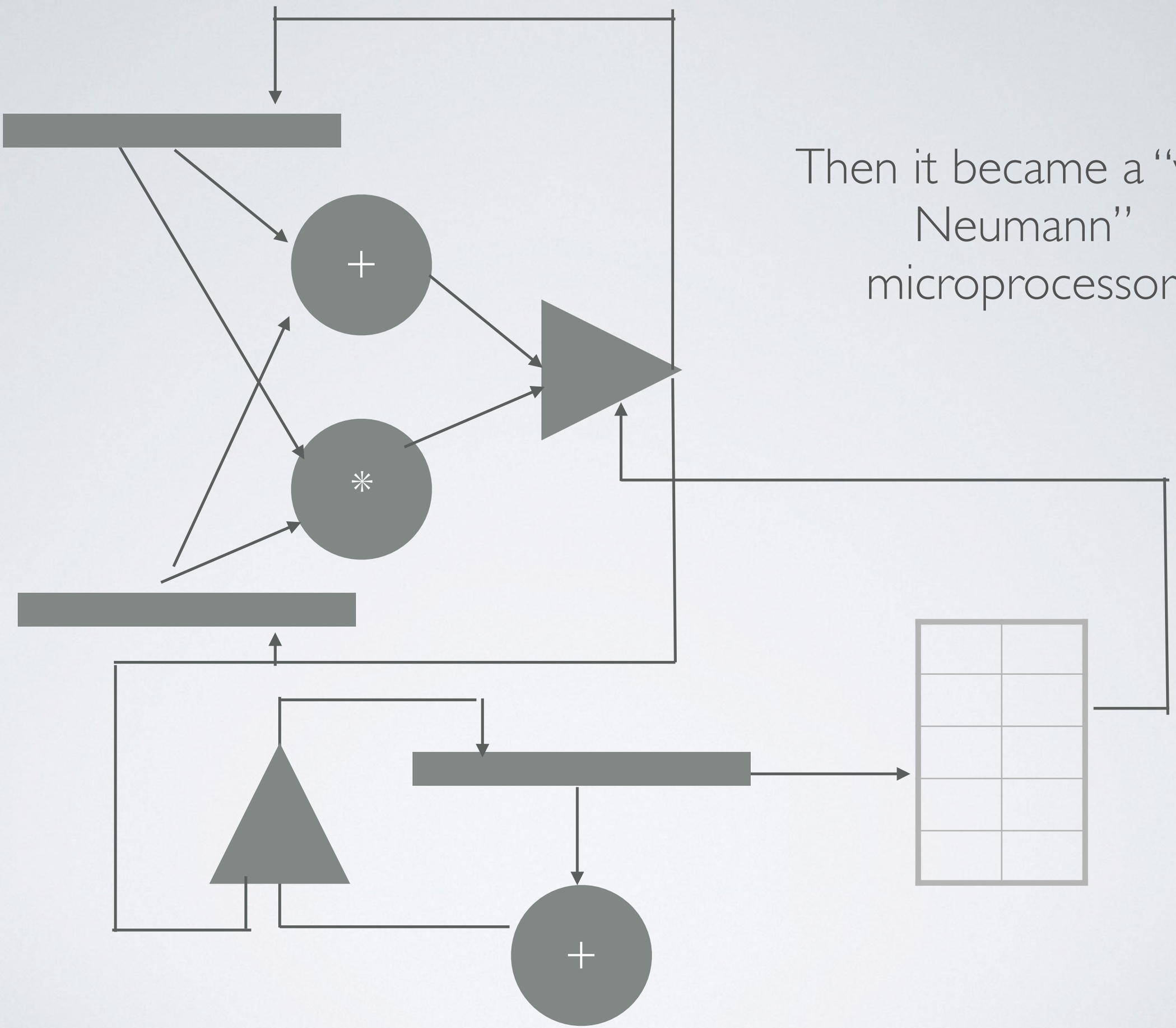




At first, ENIAC was an “FPGA”



Then it became a "von Neumann" microprocessor



But for the record…

John von Neumann

John Eckert

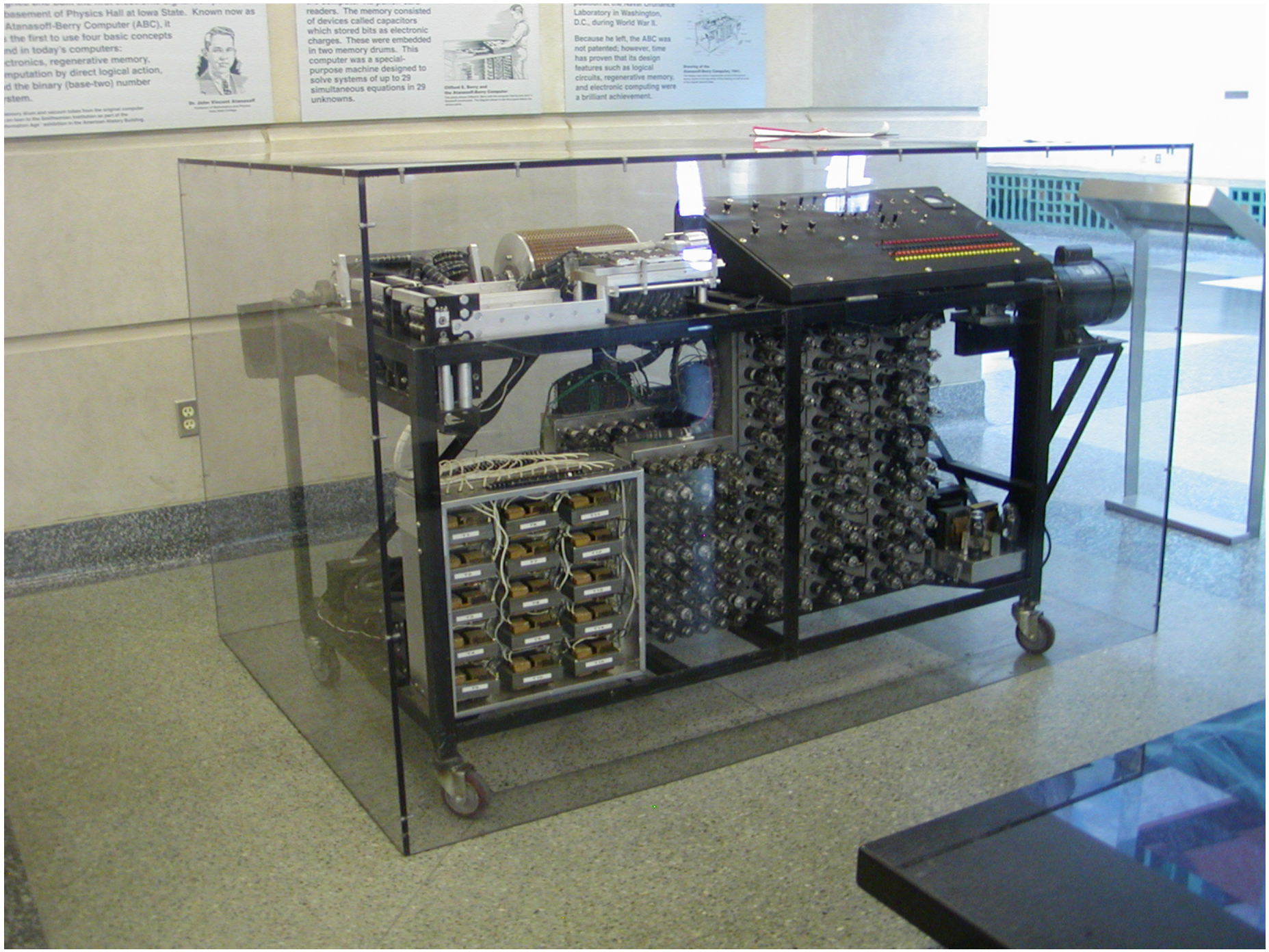
John Mauchly

Kathleen McNulty Mauchly Antonelli, Jean Jennings Bartik,
Frances Snyder Holberton, Marlyn Wescoff Meltzer,
Frances Bilas Spence and Ruth Lichterman Teitelbaum

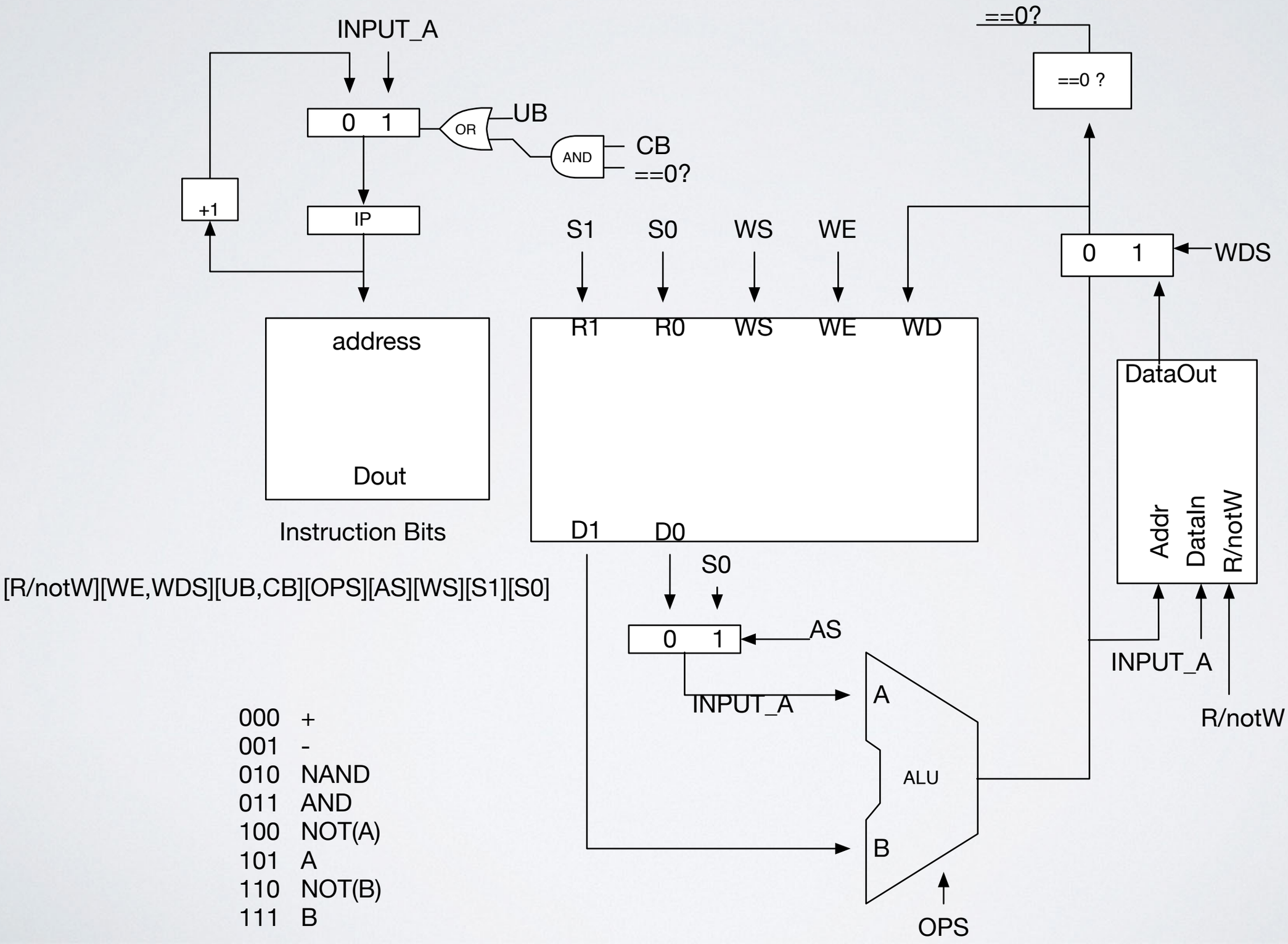
EDSAC

Maurice Wilkes

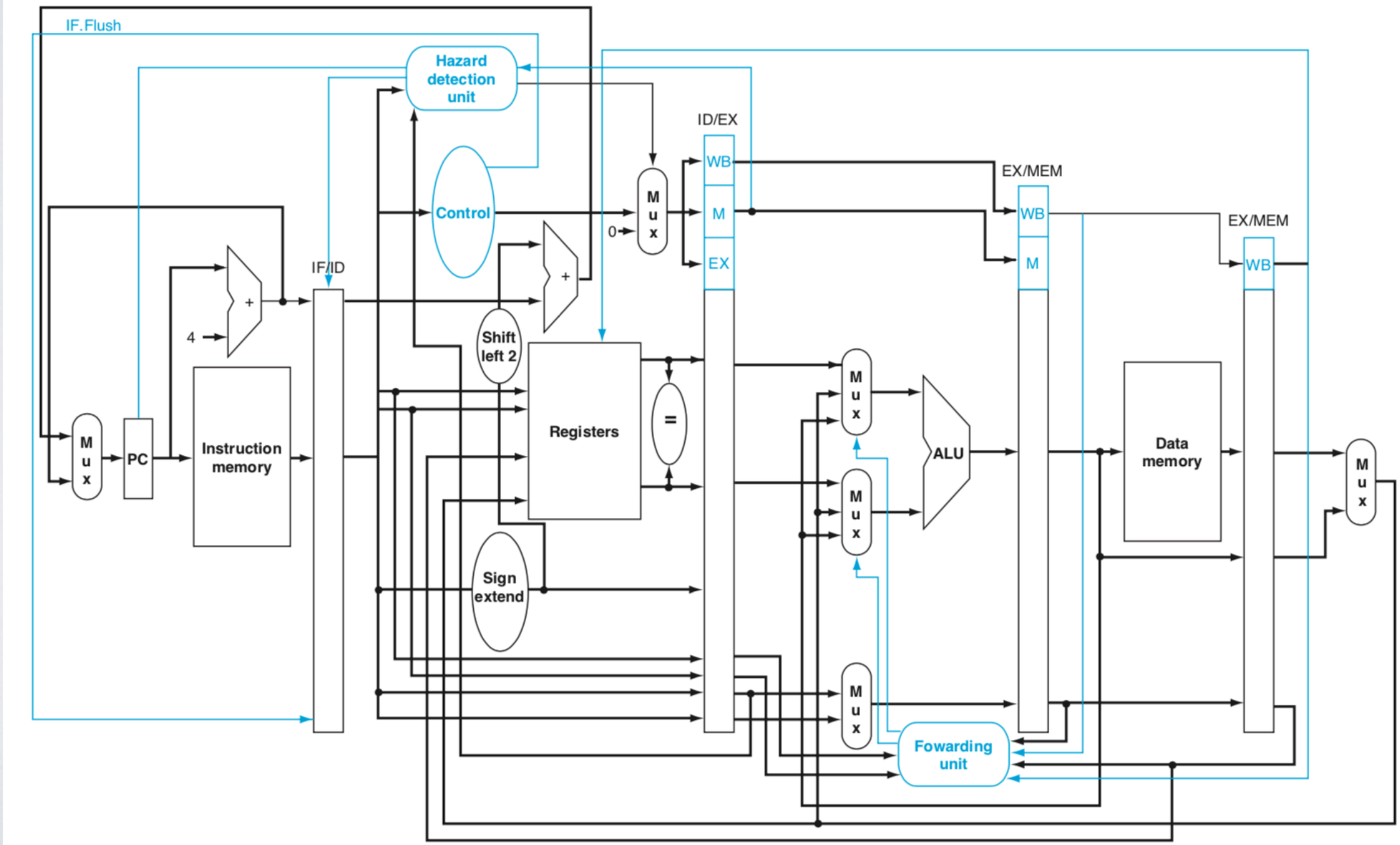
Atanasoff-Berry



FAST FORWARD ~10 YEARS



FAST FORWARD ~ 30 YEARS



…AND 50 YEARS… AND TODAY