

## EE/CSE 469 – Computer Design and Organization Winter 2018

- Instructor:** Prof. Mark Oskin (mhoskin@uw), Office hours: by appointment (email w/schedule).
- T.A.:** Eric Mullen (emullen@uw) and Xinyu Sui (suix2@uw)
- Text:** Patterson, Hennessy, *Computer Organization and Design: The Hardware/Software Interface*, ARM Edition, 2016, Morgan Kaufmann. (First ARM edition).  
**Recommended:** Frank Vahid & Roman Lysecky *Verilog for Digital Design* is also recommended.
- Topics Covered:** Introduction to computer architecture, algorithms, hardware design for various computer subsystems, CPU control unit design, memory organization, cache design, and virtual memory.
- Prerequisites:** CSE143, EE271 or CSE369. Strong knowledge of hardware design and Verilog from EE271 or CSE369 is essential.
- Assignments:** The major goals of the class are to familiarize you with basic structure of microprocessors. As part of this, students will develop a Verilog implementation of a simple RISC microprocessor based upon the ARM instruction set.  
Note that the labs **GROW SIGNIFICANTLY** in the amount of time it takes to complete them. The average time to complete the labs is expected to be:
- |                         |          |
|-------------------------|----------|
| Lab 1: Register File    | 12 hours |
| Lab 2: ALU              | 11 hours |
| Lab 3: Single-cycle CPU | 25 hours |
| Lab 4: Pipelined CPU    | 34 hours |
| Lab 5: Cache Memory     | 30 hours |
- Exams:** There will be one midterm and one final exam (March 12th, 8:30 AM. EEB0037).
- Grade:** The grade will be determined by the following approximate weights: homeworks (20%), design project (35%), midterm (20%), final exam (25%).
- Outline:** The class will have the following approximate schedule. Material may be added or dropped based on class timing and progress.  
\* Introduction to processor architecture.  
\* Assembly language programming.  
\* Computer Arithmetic.  
\* Performance measures.  
\* Processor Datapaths & Control.  
\* Pipelining.  
\* Memory hierarchy, caches, virtual memory.  
\* Advanced topics in computer architecture.

### Reading Schedule

- Week 1: 1.1 - 1.4
- Week 2: 2.1 - 2.7, 2.9 - 2.10, 2.14, Green Card
- Week 3: 3.1 - 3.3, A.5
- Week 4: 1.6 - 1.8
- Week 5: 4.1 - 4.4
- Week 6: 4.5 - 4.8
- Week 7: 5.1 - 5.4, 5.8