Consider the following series of address references:

12, 16, 40, 12, 0, 24, 20, 16, 0, 32, 36, 4, 0, 40

For each address, show the binary value, and the Cache Tag, Cache Index, and Byte Select, for each cache. Then, label each reference as a hit or miss, and show the final cache contents, for each of the following caches. Assume LRU replacement (where appropriate).

a.) Direct-mapped, 8x 4-byte blocks.

b.) Direct-mapped, 16-byte blocks, total size of 32 bytes.

c.) Two-way set associative, 4-byte blocks, total size of 32 bytes.

d.) Fully associative, 8-byte blocks, total size of 32 bytes.

		DM, 8x4-byte blocks				
Address	Binary	BS addr%4	Block # addr/4	CI block#%8	Tag block#/8	
12	1100	0	3	3	0	Miss
16	10000	0	4	4	0	Miss
40	101000	0	10	2	1	Miss
12	1100	0	3	3	0	Hit
0	0	0	0	0	0	Miss
24	11000	0	6	6	0	Miss
20	10100	0	5	5	0	Miss
16	10000	0	4	4	0	Hit
0	0	0	0	0	0	Hit
32	100000	0	8	0	1	Miss
36	100100	0	9	1	1	Miss
4	100	0	1	1	0	Miss
0	0	0	0	0	0	Miss
40	101000	0	10	2	1	Hit

Direct-mapped, 8x4 byte blocks

0	~~0-3~~ ~~32-35~~ 0-3
1	~~36-39~~ 4-7
2	40-43
3	12-15
4	16-19
5	20-23
6	24-27
7	

Address	Binary	BS addr%16	DM, 2x16-byte blocks Block # addr/16	CI block#%2	Tag block#/2	
12	1100	12	0	0	0	Miss
16	10000	0	1	1	0	Miss
40	101000	8	2	0	1	Miss
12	1100	12	0	0	0	Miss
0	0	0	0	0	0	Hit
24	11000	8	1	1	0	Hit
20	10100	4	1	1	0	Hit
16	10000	0	1	1	0	Hit
0	0	0	0	0	0	Hit
32	100000	0	2	0	1	Miss
36	100100	4	2	0	1	Hit
4	100	4	0	0	0	Miss
0	0	0	0	0	0	Hit
40	101000	8	2	0	1	Miss

Direct-mapped, 2x16byte blocks

0	~~0-15~~ ~~0-15~~ ~~32-47~~ ~~32-47~~	~~0-15~~ 32-47
1	16-31	

		2way, 2x (4x4-byte blocks)				
Address	Binary	BS addr%4	Block # addr/4	CI block#%4	Tag block#/4	
12	1100	0	3	3	0	Miss
16	10000	0	4	0	1	Miss
40	101000	0	10	2	2	Miss
12	1100	0	3	3	0	Hit
0	0	0	0	0	0	Miss
24	11000	0	6	2	1	Miss
20	10100	0	5	1	1	Miss
16	10000	0	4	0	1	Hit
0	0	0	0	0	0	Hit
32	100000	0	8	0	2	Miss
36	100100	0	9	1	2	Miss
4	100	0	1	1	0	Miss
0	0	0	0	0	0	Hit
40	101000	0	10	2	2	Hit

2-way set associative, 4-byte blocks, total of 32 bytes

0	~~16-19~~ 32-35	0-3
1	~~20-23~~ 4-7	36-39
2	40-43	24-27
3	12-15	

Note: which side any access is does not matter,
but who you replace does matter

		FA, 4x8-byte blocks				
Address	Binary	BS addr%8	Block # addr/8	CI N/A	Tag block#	
12	1100	4	1	N/A	1	Miss
16	10000	0	2	N/A	2	Miss
40	101000	0	5	N/A	5	Miss
12	1100	4	1	N/A	1	Hit
0	0	0	0	N/A	0	Miss
24	11000	0	3	N/A	3	Miss
20	10100	4	2	N/A	2	Miss
16	10000	0	2	N/A	2	Hit
0	0	0	0	N/A	0	Hit
32	100000	0	4	N/A	4	Miss
36	100100	4	4	N/A	4	Hit
4	100	4	0	N/A	0	Hit
0	0	0	0	N/A	0	Hit
40	101000	0	5	N/A	5	Miss

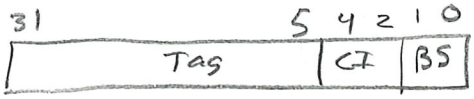
Fully Associative, 4x8-byte blocks

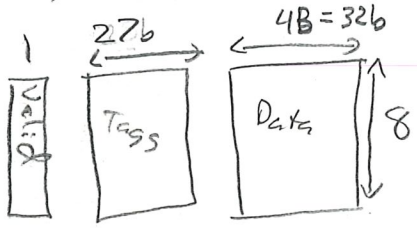
0	~~8-15~~ 32-39
1	~~16-23~~ 40-47 ~~24-31~~
2	~~40-47~~ 16-23
3	0-7

Note: where the access lands does not matter but who you replace does.

Compute the total number of bits needed to implement each of the caches from the previous problem. This number is different from the size of the cache, which usually refers to the number of bytes of data stored in the cache. The total number of bits needed to implement the cache represents the total amount of memory needed for storing all the data, tags, and valid bits. Assume 32-bit addresses.

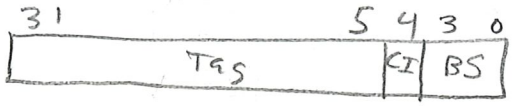
a.) DM 8×4-byte blocks Address:

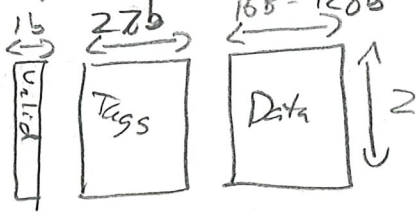




Area = 8×(1+27+32)
= 8×60 = 480b

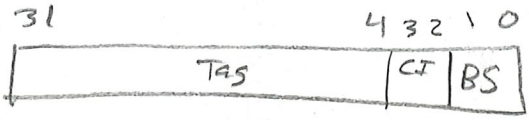
b.) DM 2×16-byte blocks Address:

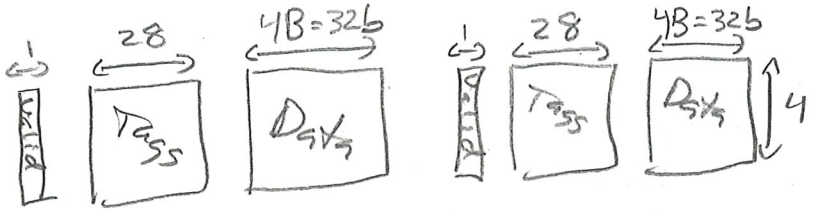




Area = 2×(1+27+128)
= 2×156 = 312b

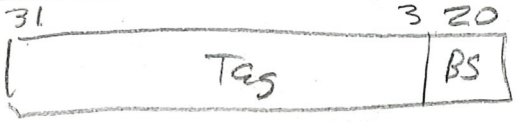
c.) 2-way, 4-byte blocks, 32bytes total Address:

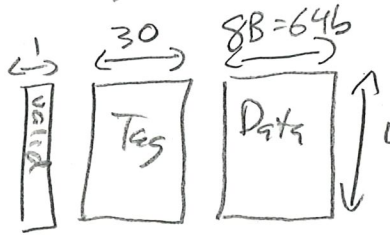




Area = 2×(4×(1+28+32))
= 8×(61) = 488b

D.) FA, 8-byte blocks, 4 blocks Address:





Area = 4×(1+30+64)
= 4×95 = 380b

You are given the following memory system:

Level	Hit Time	Hit Rate
L1	2 Cycle	95%
L2	8 Cycles	80%
Main Memory	80 Cycles	95%
Disk	50,000 Cycles	100%

For each of the following changes, indicate which level should be modified to yield the fastest system. Some changes may decrease performance over the original, but you must make the modification to one of the levels. The changes are separate (i.e. change b is on the original system, not on the one changed by change a). Note that the miss rate for the disk cannot be changed, so the right answer for c & d cannot be "disk".

a.)Decrease the hit time by a factor of 2.

b.)Increase the hit time by a factor of 2.

c.)Decrease the miss rate by a factor of 2.

d.)Increase the miss rate by a factor of 2.

$AMAT = 2 + .05 \times (8 + .2 \times (80 + .05 \times (50{,}000)))$

C.) The miss rate of the L1 (.05) affects all levels but L1 hit-time. all other miss rates have lesser impact. **L1**

D.) The miss rate of Main Memory affects only the disk, where all others affect more. **Main Memory**

$AMAT = 2 + .05 \times 8 + .05 \times .2 \times 80 + .05 \times .2 \times .05 \times 50{,}000$

$= 2 + 0.4 + 0.8 + 25$

A.) Decrease **Disk**. Biggest impact

B.) Increase **L2**. Smallest impact.