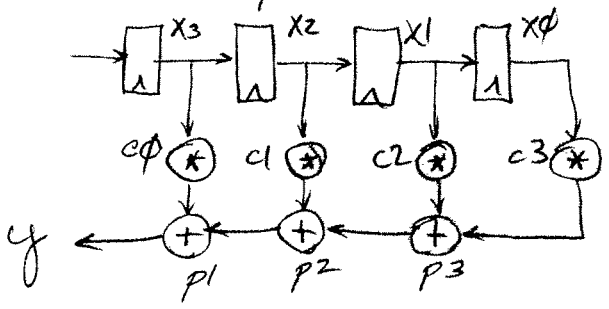
Scheduling & Time Multiplexing



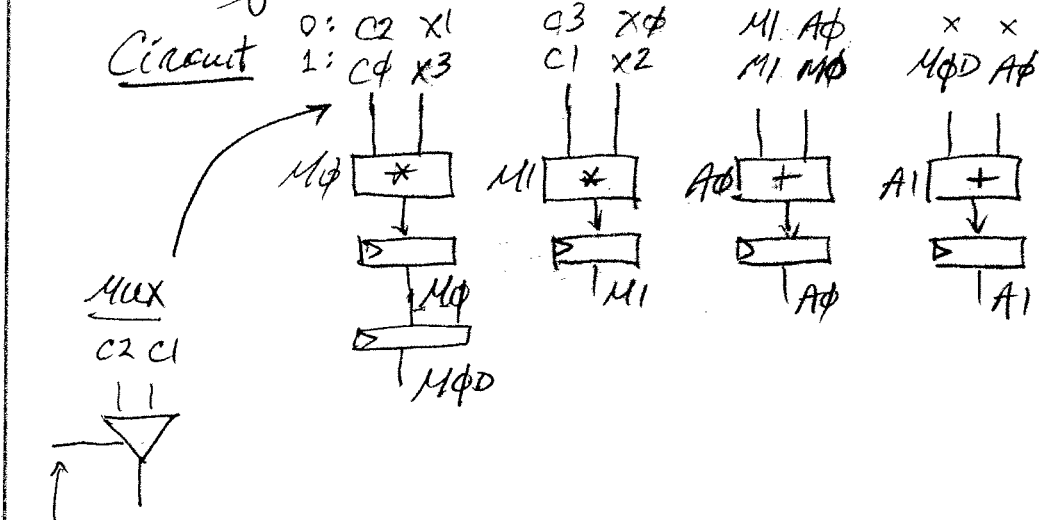
Schedule	Mφ	M1	Aφ	A1
prologue (startup)	c2	c3		
	cφ	c1	p3	
0:	c2	c3	p2	–
1:	cφ	c1	p3	p1
steady state			p2	–
epilog (shutdown)				p1

Transparent Model Schedule

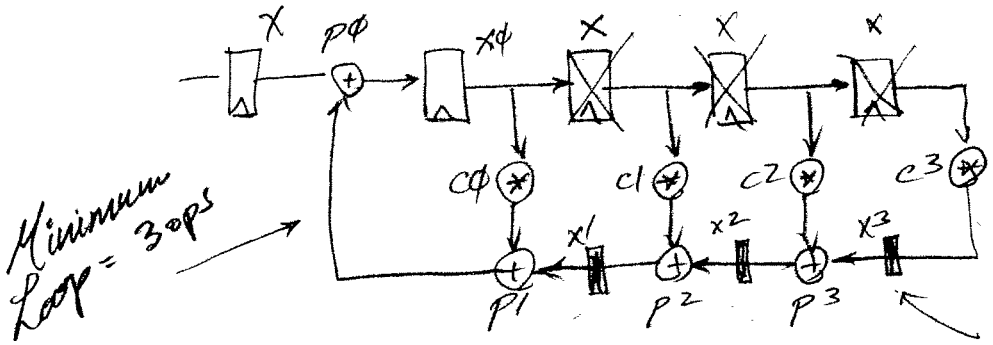
x shift register shifts every other cycle

y output is valid on cycle #1.

Circuit



Using Retiming to reduce Schedule Length



Schedule After Retiming

Schedule repeats every 3 clks