Electrical realities

- Today
  - Review basic electronics
  - Some real-world examples
  - Fixed-function logic
  - Oscilloscopes

Basic electronics

- What you should know
  - Voltage and current
  - Resistors
  - Capacitors
  - Inductors
  - Time constants
  - Bandwidth and risetime

Current and voltage

- Current is the flow of charge
  - Assume positively charged particles
  - Real physical current is negatively charged electrons
  - Units are amps; we will use mA (10^-3 A) or µA (10^-6 A)
  - 1 amp = 1 coulomb/sec
  - 1 electron has a charge of ~1.6x10^-19 coulombs

- Voltage is a measure of potential energy
  - Work that can be done by the electrons
  - Must always have a reference; we will use ground
  - Units are volts; we will use V or mV (10^-3 V)

Energy and power

- Energy is measured in joules
  - Raising the potential of 1 coulomb of (positive) charge by 1 V takes 1 joule of energy

- Power is measured in Watts
  - Energy per unit time
  - Joules/second
  - In a circuit, P = IV
  - in Watts = Joules/second

Resistors

- Ohm’s law: \( v = iR \)
- Energy: \( \int vdt = \int i^2 R dt = \int i^2 R t \) (assuming \( i \) is constant = \( I \))
  - \( i \) = current (time varying), \( I \) = current (d.c.)
  - \( v \) = voltage; \( R \) = resistance
- Power: \( \frac{dE}{dt} = i^2 R \)

Resistors (con’t)

- Resistors in series
- Resistors in parallel

\[
\begin{align*}
R_{eq} &= R_1 + R_2 \\
\frac{1}{R_{eq}} &= \frac{1}{R_1} + \frac{1}{R_2}
\end{align*}
\]
Capacitors

\[ q = CV \]
\[ i = \frac{dq}{dt} = C \frac{dV}{dt} \]

Energy:
\[ E = \int i dt = \int CV \frac{dV}{dt} dt = C \int V \frac{dV}{dt} = \frac{1}{2} CV^2 \]

- \( q \) = charge, \( i \) = current
- \( v \) = voltage, \( C \) = capacitance

Power:
\[ P = \frac{dE}{dt} = 0 \]
- Capacitors are dissipationless

Capacitors (con't)

\[ V = \frac{1}{C_1} q_1 + \frac{1}{C_2} q_2 \]
\[ C_{eq} = \frac{1}{C_1} + \frac{1}{C_2} \]

Inductors

\[ \Phi = LI \]
\[ V = \frac{d\Phi}{dt} = LI \]

Energy:
\[ E = \int i dt = L \int \frac{d\Phi}{dt} dt = \frac{1}{2} LI^2 \]

- \( \Phi \) = flux, \( v \) = voltage
- \( i \) = current, \( L \) = inductance

Power:
\[ P = \frac{dE}{dt} = 0 \]
- Inductors are dissipationless

Inductors (con't)

\[ I_{eq} = I_1 + I_2 \]
\[ L_{eq} = L_1 + L_2 \]

Time constants

\[ V_n = V_i + V_{out} \]
\[ i = IC \frac{dV_{out}}{dt} \]
\[ V_n = R_i + V_{out} \]
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\[ V_n = V_i + R \frac{dV_{out}}{dt} \]
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Synchronous (clocked) circuits have huge transient supply currents
Logic elements switch simultaneously
Peak current is orders of magnitude larger than static current
Wire resistance and inductance causes transient voltage bounce on power bus

CMOS inverter switching threshold and short-circuit current

Transistor circuits
Power and ground bounce
- Bus drops reduce logic-gate voltages
  - Switching currents are smaller
  - Logic gates are slower
- Bus drops reduce noise margins
  - Especially for low-voltage logic
  - Can cause bit errors
- Inverter has less output current
- Bus drop can cause M to erroneously discharge node X

Example 1
- You must test a high-speed FPGA
  - Output rise times (10% – 90%) are 2ns
- What is the minimum scope bandwidth?
  - For you to see rising edges reliably

Example 2
- An inverter drives a 50pF load capacitor at 100MHz
  - How much power does it dissipate driving the load?

\[
\text{Power} = C \cdot V_{dd}^2 / f = \left(5 \times 10^{-12} \text{F}\right) \left(5 \text{V}\right)^2 \left(100 \times 10^6 \text{Hz}\right) = 125 \text{mW}
\]

Example 3
- A processor IC has a transient (surge) current of 12A every time the clock switches. The surge risetime is 2ns.
  - The PCB trace resistance is 0.15Ω
  - What is the resistive voltage drop
    \[ V_R = I \cdot R = (12 \text{A}) \left(0.15 \Omega\right) = 180 \text{mV} \]
  - The chip uses 20 \( V_{dd} \) bondwires, each with an inductance of 1nH
  - What is the inductive voltage drop
    \[ V_L = \frac{dI}{dt} \left(1 \text{H}\right) \left(12 \text{A}\right) \left(2 \text{ns}\right) = 300 \text{mV} \]

IC Logic levels, voltage, & definitions
- Logic gates operate on real physical voltages
  - "1" = high voltage
  - "0" = low voltage
- We cannot guarantee precise voltages, so we allow a range
  - \( V_{oh} \) = minimum output voltage high
  - \( V_{oh} \) = maximum output voltage low
  - Guaranteed logic swing = \( V_{oh} - V_{il} \)
  - \( V_{ih} \) = minimum input voltage high
  - \( V_{il} \) = maximum input voltage low
  - Noise margin: \( NM_L = V_{il} - V_{oh} \)
  - \( NM_H = V_{oh} - V_{ih} \)

TTL and CMOS logic levels
- TTL = Transistor-transistor logic (bipolar transistors)
- CMOS = Complementary metal oxide semiconductor
- TTL I/O are closer to ground than CMOS
- Logic families not 100% compatible
- More about this later
TTL/CMOS Transfer Characteristics

More definitions

- **Propagation delay**: The delay through a gate
  - Measured at the 50% points on the input and output waveforms
  - Has a range: min/typical/max
  - Depends on the fanout
  - The number of loads the gate drives
  - Your design must work over the entire delay range

- **Rise and fall times**: Time for a signal to transition
  - Typically measured at 10% to 90% of the logic swing
  - Sometimes at 20% to 80%

- **Pulse width**: time that an output stays high
  - Duty cycle \( \frac{(pulse \ width)}{(pulse \ period)} \)
  - Frequency \( \frac{1}{(pulse \ period)} \)
Comparing logic families

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>LS</th>
<th>ACT</th>
<th>NMOS</th>
<th>CMOS</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Voltage Range</td>
<td>$V_{DD/SS}$</td>
<td>5.0 ± 5.0</td>
<td>5.0 ± 5.0</td>
<td>5.0 ± 0.5</td>
<td>5.0 ± 0.0</td>
<td>V</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>$T_A$</td>
<td>0 °C to 70 °C</td>
<td>0 °C to 70 °C</td>
<td>-40 °C to 85 °C</td>
<td>-25 °C to 85 °C</td>
<td>°C</td>
</tr>
<tr>
<td>Input Voltage (Min)</td>
<td>$V_{IN}$</td>
<td>0.0</td>
<td>0.8</td>
<td>1.0</td>
<td>1.0</td>
<td>V</td>
</tr>
<tr>
<td>Output Voltage (Max)</td>
<td>$V_{O}$</td>
<td>0.8</td>
<td>0.8</td>
<td>1.0</td>
<td>1.0</td>
<td>V</td>
</tr>
<tr>
<td>Output Current</td>
<td>$I_{O}$</td>
<td>20 mA</td>
<td>30 mA</td>
<td>50 mA</td>
<td>50 mA</td>
<td>A</td>
</tr>
<tr>
<td>Input Current</td>
<td>$I_{C}$</td>
<td>10 mA</td>
<td>-40 mA</td>
<td>-40 mA</td>
<td>-35 mA</td>
<td>A</td>
</tr>
<tr>
<td>Specifications</td>
<td>$V_{OH}$</td>
<td>4.0 V</td>
<td>2.4 V</td>
<td>2.4 V</td>
<td>2.4 V</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>0.0 V</td>
<td>0.0 V</td>
<td>0.0 V</td>
<td>0.0 V</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>DC Noise Margin</td>
<td>Low-High</td>
<td>150 mV</td>
<td>200 mV</td>
<td>150 mV</td>
<td>200 mV</td>
<td>V</td>
</tr>
<tr>
<td>DC Power</td>
<td>-</td>
<td>35 W</td>
<td>25 W</td>
<td>25 W</td>
<td>25 W</td>
<td>W</td>
</tr>
</tbody>
</table>

Electrical realities

- ICs draw lots of current when switching
  - Power supply is typically far away
  - Many nanoseconds of wire
  - The chip supply voltage will drop
  - Degrading the outputs
- Add decoupling
  - A capacitor from $V_{DD}$ to Gnd
  - Right at the chip pins
  - Keeps voltage from dropping
  - $C = CV/I$
- Tie unused chip inputs to gnd
  - Prevents random switching

Electrostatic discharge (ESD)

- Triboelectric charging: Charge transfer due to the contact and separation of materials
  - Electrons transfer from one material to the other
  - You can acquire 5 – 15 thousands of volts of static charge
  - By walking on carpet or moving your clothes or...
- ESD: Charge transfer between bodies at different potentials
  - You feel a shock when you touch something
  - This shock will kill a chip
- Most ICs have input protection
  - But only good to about 2000V

Eliminating ESD

- Design for ESD
  - Use protection circuitry
  - Use proper packaging
- Reduce charge generation
  - Wear cotton clothing
  - Keep humidity up
  - Use conductive packaging
- Dissipate charge
  - Use ground straps, ground mats, etc.
  - Ground yourself before touching an IC

Oscilloscopes

- Measure voltage as a function of time
  - Vertical scale is in volts/division
  - Set using scale knob
  - Horizontal scale is time/division
  - Set using timebase
- You tell the scope when to acquire data
  - You trigger the scope
  - Tell it to capture a 10,000 point waveform (Normal mode)
  - The trigger can be any event
  - Another signal
  - Some feature of your signal
  - The trigger must be correlated with your waveform
  - Else successive acquisitions will look random

ESD damage

- Due to poor handling practices
  - Usually people not discharging themselves before touching chips
- Failure types
  - Catastrophic
    - Chip dies immediately
  - Latent defects
    - Chip dies early in life

SEM photo of chip failure due to electrical overstress
http://www.sem-lab.com/
Triggering oscilloscopes (con't)

- Normal trigger mode
  - Scope triggers continuously
- Pretriggering and delay
  - You tell the scope when to take data relative to the trigger
- Single-shot acquisition
  - You tell the scope to trigger once and stop
- Trigger icons help you
  - Trigger-position icon: Shows the trigger location in the waveform
  - Trigger-level icon: Shows the trigger voltage level on the waveform
  - Waveform-record icon: Shows the trigger location in the record

Oscilloscope features

- Measurement
  - Cursors measure voltage, time, frequency
  - Autoset configures the scope for you
- Signal processing
  - Averaging multiple waveforms reduces noise
  - Envelope captures maximum variation of a signal
  - Can do math on waveforms

Oscilloscope probing

- Probes have 2 terminals
  - Center conductor: Signal
  - Outer conductor: Ground
- You must supply a good ground
  - Voltage reference for the scope
  - Return path for current that goes up the probe
    - Recall Kirchoff's laws
- Our scopes have 2 or 4 channels
  - Can probe 2 or 4 signals simultaneously
  - They must be related in frequency