Introduction to Re-usable IP and MicroBlaze™ architecture

32-bit RISC soft processor core for Xilinx FPGAs

Productivity Problem
- Designer = 100 gates/day, 10 lines tested-debugged verilog
- Design = 200,000 gates, optimum design team = 2
- Project = 1000 days, almost 3 years!
- Management expects project done in a year or less
- Result = Big Problem!
- Solutions?

Productivity Increase
- Bigger Design team
- Coffman’s Law
- Individual designer must produce more code
- Each line of code represents more gates
- Reuse designs
  - Libraries
  - Reuse old projects
  - Buy IP (Intellectual Property)

Structural Verilog
```verilog
module xor_gate (out, a, b);
  input a, b;
  output out;
  wire abar, bbar, t1, t2;
  not not0 (abar, a);
  not not1 (bbar, b);
  and and1 (t1, abar, b);
  and and2 (t2, bbar, a);
  or or1 (out, t1, t2);
endmodule
```
8 basic gates (keywords):
- and, or, nand, nor
- buf, not, xor, xnor

Behavioral Verilog
- Describe circuit behavior
- Not implementation

```verilog
module full_adder (Sum, Cout, A, B, Cin);
  input A, B, Cin;
  output Sum, Cout;
  assign (Cout, Sum) = A + B + Cin;
endmodule

(Cout, Sum) is a concatenation
What is MicroBlaze?

- It's a soft processor, around 900 LUTs
- RISC Architecture
- 32-bit, 32 x 32 general purpose registers
- Supported in Virtex/EII/IIPro, Spartan-III/IIE

MicroBlaze features

- Thirty-two 32-bit general purpose registers
- 32-bit instruction word with three operands and two addressing modes
- Separate 32-bit instruction and data buses that conform to IBM's OBP (On-chip Peripheral Bus) specification
- Separate 32-bit instruction and data buses with direct connection to on-chip block RAM through a LMB (Local Memory Bus)
- 32-bit address bus
- Single issue pipeline
- Instruction and data cache
- Hardware debug logic
- FSL (Fast Simplex Link) support

Instruction pipeline

<table>
<thead>
<tr>
<th>Instruction</th>
<th>cycle 1</th>
<th>cycle 2</th>
<th>cycle 3</th>
<th>cycle 4</th>
<th>cycle 5</th>
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<tr>
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<td>Fetch</td>
<td>Decoded</td>
<td>Execute</td>
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Big-Endian Data Type

```c
int i;
char c[ ];
short s[ ];
```

Embedded Development Kit (EDK)

- All encompassing design environment for Virtex-II Pro PowerPC™ and MicroBlaze based embedded systems in Xilinx FPGAs
- Integration of mature FPGA and embedded tools with innovative IP generation and customization tools
- Delivery vehicle for Processor IP

EDK System Design Comprehensive Tool Chain
More on MicroBlaze ...

- Harvard Architecture
- Configurable instruction cache, data cache soon
- Non-intrusive JTAG debug
- Support for 2 buses:
  - LMB (Local Memory Bus) - 1 clock cycle latency, connects to BRAM
  - OPB (On-chip Peripheral Bus) - part of the IBM CoreConnect™ standard, connects to other peripheral
    “Portable” IP between PPC and MB
- Big endian, same as PowerPC PPC405

MicroBlaze Interrupts and Exceptions

- Interrupt handling
  - 1 Interrupt port
    - 32+ interrupts and masking supported through interrupt controller(s)
- Exception handling
  - No exceptions generated in Virtex-II versions
  - One in Virtex/E and Spartan-II versions for MUL instruction

Software Tools

- GNU tool chain
- GCC - GNU Compiler Collection
- GDB - The GNU debugger
  - Source code debugging
  - Debug either C or assembly code
- XMD - Xilinx Microprocessor Debug utility
  - Separate Process
  - Provides cycle accurate program execution data
  - Supported targets: simulator, hardware board

Software - XMD

- Interfaces GDB to a “target”
- Allows hardware debug without a ROM monitor or reduces debug logic by using xmd-stub (ROM monitor)
- Offers a variety of simulation targets
  - Cycle accurate simulator
  - Real hardware board interface via UART or MDM
- Includes remote debugging capability

Example MicroBlaze System

Processor IP (HW/SW)

Infrastructure (includes Device Drivers)

- MicroBlaze CPU
- LMB2OPB Bridge
- PLB Arbiter & Bus Structure (PLB_V3H)
- OPB Arbiter & Bus Structure (OPB_V20)
- DCR Bus Structure (DCR_V29)
- PLB2OPB Bridge
- OPB2PLB Bridge
- OPB2OPB Bridge – Lite
- OPB2DCR Bridge
- System Reset Module
- BSP Generator (SW only)
- ML3 VxWorks BSP (SW only)
- Memory Test Utility (SW only)

OPB SPFI Modules (includes Device Drivers)

- PLB SPFI
  - PLB SPFI Slave Attachment
  - PLB SPFI Master Attachment
  - PLB SPFI Master Adapter
  - PLB SPFI Slave Adapter
  - PLB SPFI Master Interface
  - PLB SPFI Slave Interface
  - PLB SPFI Master Compiler
  - PLB SPFI Slave Compiler
  - PLB SPFI Master Debugger
  - PLB SPFI Slave Debugger
Processor IP (HW/SW)

Memory Interface (includes Device Drivers & Memory Maps)
- PS2 DRAM (Flash, SRAM, and 2D)
- PS2 BRAM Controller
- PS2 DRAM Controller
- PS2 SDRAM Controller
- ORS DRAM (Flash, SRAM, and 2D)
- ORS BRAM Controller
- ORS DRAM Controller
- ORS SDRAM Controller
- ORS SystemI2C
- LNS BRAM Controller

Peripherals (includes Device Drivers & RTOS Adapt. Layers)
- ORS Single Channel HICL Controller
- ORS – HIC Full Bridge
- ORS 10/100 MBit Ethernet
- ORS 10/100 MBit Ethernet - Lite
- ORS ATM UpLink Level 2 Slave
- ORS ATM UpLink Level 2 Master

Peripherals (continued)
- ORS 32-bit Master & Slave
- ORS UART-16550
- ORS UART-16450
- ORS UART-1 Lite
- ORS 80C51 UART
- ORS Interrupt Controller
- ORS Timebase/Watch Dog Timer
- ORS Timer Counter
- ORS GPIO
- PS2 Gig Ethernet
- PS2 RapidIO
- PS2 UART-16550
- PS2 UART-16450
- PS2 ATM UpLink Level 2 Slave
- PS2 ATM UpLink Level 2 Master
- PS2 ATM UpLink Level 3 Slave
- PS2 ATM UpLink Level 3 Master
- DCR Interlink Controller

The Benefits of Parameterization

Example: OPB Arbiter

| RAM_MASTER | PROTOCOL INTERFACE | DRAM_PRIORITY | PARM | BUS GRANTS | RAM | LUT | Func
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<td>1</td>
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</tbody>
</table>

- Significantly increases performance or saves area
- Only include what you need
- This can only be accomplished in a programmable system

Buses and Arbiters

- PLB
  - Arbitration for up to 16 masters
  - 64-bit and 32-bit masters and slaves
  - SIM PLB compliant
- OBP
  - Includes arbiter with dynamic or fixed priorities and bus parking
  - Parameterized I/O for any number of masters or slaves
  - SIM OPB compliant
- DCR
  - Supports one master and multiple slaves
  - Daisy chain connections for the DCR data bus
  - Required OR function of the DCR slaves’ acknowledge signal
- LBIM
  - MicroBlaze single-master Local Memory Bus

System Infrastructure

- Hardware IP
  - Common PowerPC and MicroBlaze peripherals
  - Peripherals are common across bus types
  - Parameterize for optimal functionality, optimal FPGA usage
- IP Interface (IPIF) provides common hardware blocks
- Software IP (Device Drivers)
  - Common across processors and operating systems

Full IP Interface (IPIF)

- Consists of 8 modules
  - Each module is selectable and parameterizable
  - Automatically configures a core to the processor bus
  - 890 PLB classes
  - 3rd Party IP Cores
  - Customer proprietary cores and external devices
  - OPB & PLB supported
  - Bus independent bus cores and associated Device Drivers
- IPF will be added to other LogiCOREs

Bridges

- PLB to OPB
  - Decode up to 4 different address ranges
  - 32-bit or 64-bit PLB slave, 32-bit OPB master
  - Burst and non-burst transfers, cache-line transactions
- OPB to PLB
  - 64-bit PLB master, 32-bit OPB slave
  - Burst and non-burst transfers, cache-line transactions
  - BEI and BEAR
- OPB (slave) to DCR (master)
- Memory mapped DCR control
- OPB to OPB
  - Allows further OPB partitioning
**More System Cores**
- Processor System Reset
  - Asynchronous external reset input is synchronized with clock
  - Selectable active high or active low reset
  - DCM Locked input
  - Sequencing of reset signals coming out of reset:
    1. First - bus structures come out of reset
    2. Second - Peripheral(s) come out of reset 16 clocks later
    3. Third - the CPU(s) come out of reset 16 clocks after the peripherals
- JTAG Controller
  - Wrapper for the JTAGPPC primitive.
  - Enables the PowerPC’s debug port to be connected to the FPGA JTAG chain
  - IP/EP User Core Templates
  - Convenient way to add user core to OPB or PLB

**Timer / Counter**
- Supports 32-bit OPB v2.0 bus interface
- Two programmable interval timers with interrupt, compare, and capture capabilities
- Programmable counter width
- One Pulse Width Modulation (PWM) output

**Watchdog Timer / Timebase**
- Supports 32-bit bus interfaces
- Watchdog timer (WDT) with selectable timeout period and interrupt
- Two-phase WDT expiration scheme
- Configurable WDT enable: enable-once or enable-disable
- WDT Reset Status (was the last reset caused by the WDT?)
- One 32-bit free-running timebase counter with rollover interrupt

**Interrupt Controller**
- Number of interrupt inputs is configurable up to the width of the data bus width
- Interrupt controllers can be easily cascaded to provide additional interrupt inputs
- Master Enable Register for disabling the interrupt request output
- Each input is configurable for edge or level sensitivity
  - rising or falling, active high or active low
- Output interrupt request pin is configurable for edge or level generation

**UART 16550 / 16450 / Lite**
- Register compatible with industry standard 16550/16450
- 5, 6, 7 or 8 bits per character
- Odd, even or no parity detection and generation
- 1, 1.5 or 2 stop bit detection and generation
- Internal baud rate generator and separate RX clock input
- Modem control functions
- Prioritized transmit, receive, line status & modem control interrupts
- Internal loop back diagnostic functionality
- Independent 16 word transmit and receive FIFOs

**IIC**
- 2-wire (SDA and SCL) serial interface
- Master/Slave protocol
- Multi-master operation with collision detection and arbitration
- Bus busy detection
- Fast Mode 400 KHz or Standard Mode 100 KHz operation
- 7 Bit, 10 Bit, and General Call addressing
- Transmit and Receive FIFOs - 16 bytes deep
- Bus throttling
### SPI
- 4-wire serial interface (MOSI, MISO, SCK, and SS)
- Master or slave modes supported
- Multi-master environment supported (requires tri-state drivers and software arbitration for possible conflict)
- Multi-slave environment supported (requires additional decoding and slave select signals)
- Programmable clock phase and polarity
- Optional transmit and receive FIFOs
- Local loopback capability for testing

### Ethernet 10/100 MAC
- 32-bit OPB master and slave interfaces
- Media Independent Interface (MII) for connection to external 10/100 Mbps PHY Transceivers
- Full and half duplex modes of operation
- Supports unicast, multicast, broadcast, and promiscuous addressing
- Provides auto or manual source address, pad, and Frame Check Sequence

### Ethernet 10/100 MAC (cont)
- Simple DMA and Scatter/Gather DMA architecture for low processor and bus utilization, as well as a simple memory-mapped direct I/O interface
- Independent 2K to 32K transmit and receive FIFOs
- Supports MII management control writes and reads with MII PHYs
- Supports VLAN and Pause frames
- Internal loopback mode

### 1 Gigabit MAC
- 64-bit PLB master and slave interfaces
- GMII for connection to external PHY Transceivers
- Optional PCS function with Ten Bit Interface (TBI) to external PHY devices
- Option PCS/PMA functions with SerDes interface to external transceiver devices for reduced signal count
- Full duplex only
- Provides auto or manual source address, pad, and Frame Check Sequence

### 1 Gigabit MAC (cont)
- Simple DMA and Scatter/Gather DMA architecture for low processor and bus utilization, as well as a simple memory-mapped direct I/O interface
- Independent, depth-configurable TX and RX FIFOs
- Supports MII management control writes and reads with MII PHYs
- Jumbo frame and VLAN frame support
- Internal loopback mode

### Single Channel HDLC
- Support for a single full duplex HDLC channel
- Selectable 8/16 bit address receive address detection, receive frame address discard, and broadcast address detection
- Selectable 16 bit (CRC-CCITT) or 32 bit (CRC-32) frame check sequence
- Flag sharing between back to back frames
- Data rates up to OPB_CLK frequency
**Single Channel HDLC (cont)**
- Simple DMA and Scatter/Gather DMA architecture for low processor and bus utilization, as well as a simple memory-mapped direct I/O interface
- Independent, depth-configurable TX and RX FIFOs
- Selectable broadcast address detection and receive frame address discard
- Independent RX and TX data rates

**ATM Utopia Level 2**
- UTOPIA Level 2 master or slave interface
- UTOPIA interface data path of 8 or 16 bits
- Single channel VPJ/VCI service and checking in received cells
- Header error check (HEC) generation and checking
- Parity generation and checking
- Selectively prepend headers to transmit cells, pass entire received cells or payloads only, and transfer 48 byte ATM payloads only

**ATM Utopia Level 2 (cont)**
- Simple DMA and Scatter/Gather DMA architecture for low processor and bus utilization, as well as a simple memory-mapped direct I/O interface
- Independent, depth-configurable TX and RX FIFOs
- Interface throughput up to 622 Mbps (OC12)
- Internal loopback mode

**OPB-PCI Bridge**
- 33/66 MHz, 32-bit PCI buses
- Full bridge functionality
  - OPB Master read/write of a remote PCI target (both single and burst)
  - PCI Initiator read/write of a remote OPB slave (both single and multiple)
- Supports up to 3 PCI devices with unique memory PCI memory space
- Supports up to 6 OPB devices with unique memory OPB memory space
- PCI and OPB clocks can be totally independent

**System ACE Controller**
- Used in conjunction with System ACE CompactFlash Solution to provide a System ACE memory solution.
- System ACE Microprocessor Interface ( MPU)
  - Read/Write from or to a CompactFlash device
  - MPU provides a clock for proper synchronization
- ACE Flash (Xilinx-supplied Flash Cards)
  - Densities of 128 MBits and 256 MBits
  - CompactFlash Type 1 form factor
    - Supports any standard CompactFlash module, or IBM microdrives up to 8 GBs, all with the same form factor.
- Handles byte, half-word, and word transfers

**GPIO**
- OPB V2.0 bus interface with byte-enable support
- Supports 32-bit bus interface
- Each GPIO bit dynamically programmable as input or output
- Number of GPIO bits configurable up to size of data bus interface
- Can be configured as inputs-only to reduce resource utilization
Memory Controllers
- PLB and OPB interfaces
- External Memory Controller
  - Synchronous Memory (ZBT)
  - Asynchronous Memory (SRAM, Flash)
- Internal Block Memory (BRAM) Controllers
- DDR and SDRAM

Creating a Simple MicroBlaze System with EDK

Design Flow
- Design Entry with Xilinx Platform Studio
- Generate system netlist with XPS
- Generate hardware bitstream with XPS
- Download and sanity check design with XPS and XMD

Simple MicroBlaze System Block Diagram