Origin of FPGAs

ADAPTED FROM:
The Design Warrior’s Guide to FPGAs
Devices, Tools, and Flows. ISBN 0750676043
Copyright © 2004 Mentor Graphics Corp.
(www.mentor.com)

Technology timeline

Programmable Logic Devices

Some Combinational Logic

Programmed PROM

Unprogrammed PROM
Unprogrammed PLA

Programmed PLA

Unprogrammed PAL

Generic CPLD Structure

Using Programmable Multiplexers

Programming a Physical PLD
Different Types of ASICs

ASICS

- Gate Arrays
- Structured ASICs
- Standard Cell
- Full Custom

Increasing complexity

Structured ASIC tiles

(a) Gate, mux, and flop-based
(b) LUT and flop-based

Examples of simple gate array basic cells

(a) Pure CMOS basic cell
(b) BiCMOS basic cell

Generic structured ASIC

- Prefabricated I/O, cones, etc.
- Embedded RAM
- Sea-of-tiles

Channeled gate array architectures

(a) Single-column arrays
(b) Dual-column arrays

The Gap–FPGAs

- PLDs
- SPLDs
- CPLDs

ASICS

- Gate Arrays
- Structured ASICs
- Standard Cell
- Full Custom

*Not available until early 1980s
Function and Table

Required function

\[
\begin{align*}
\text{AND} & \quad a \quad \& \\ \text{OR} & \quad b \\ c & \quad y = (a \& b) \lor c
\end{align*}
\]

Truth table

<table>
<thead>
<tr>
<th>a</th>
<th>b</th>
<th>c</th>
<th>y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

A Multifaceted LUT

Transmission-based LUT

Transmission gate (active low)

Transmission gate (active high)

SRAM cells

Xilinx Logic Cell

16-bit SR

16 x 1 RAM

4-input LUT

MUX

Flip-flop

Clock

Clock enable

Set/reset

Xilinx slice

Slice

16-bit SR

16 x 1 RAM

4-input LUT

MUX

Logic Cell (LC)

LUT

MUX

REG

16-bit SR

16 x 1 RAM

4-input LUT

MUX

Logic Cell (LC)

LUT

MUX

REG

Configuration cells linked in a chain

From the previous cell in the chain

SRAM cells

To the next cell in the chain
**Deskewing**

- Clock signal from outside world
- Special clock pin and pad
- Daughter clock (monitored downstream of the clock manager) fed back to special input
- De-skewed daughter clocks used to drive internal clock trees or output pins
- Main (mother) clock
- Untreated daughter clock
- De-skewed daughter clock

---

**General-purpose IO banks**

- General-purpose I/O banks 0 through 7

---

**XCV 1000 – Pin Layout**

- Rows A, B, A' are available for input/output
- Any pin with the User IO label (see Package Pin Legend) is available for use.