Features

- Pin and Function Compatible with CY7C1019BV33
- High speed
  - $t_{AA} = 8, 10, 12, 15$ ns
- CMOS for optimum speed/power
- Data Retention at 2.0V
- Center power/ground pinout
- Automatic power-down when deselected
- Easy memory expansion with CE and OE options
- Available in 32-pin TSOP II and 400-mil SOJ package

Functional Description

The CY7C1019CV33 is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable (CE), an active LOW Output Enable (OE), and three-state drivers. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

Writing to the device is accomplished by taking Chip Enable (CE) and Write Enable (WE) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_16).

Reading from the device is accomplished by taking Chip Enable (CE) and Output Enable (OE) LOW while forcing Write Enable (WE) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected (CE HIGH), the outputs are disabled (OE HIGH), or during a write operation (CE LOW, and WE LOW).

The CY7C1019CV33 is available in a standard 32-pin TSOP II and 400-mil-wide SOJ.
Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ........................................... –65°C to +150°C
Ambient Temperature with Power Applied.......................... –55°C to +125°C
Supply Voltage on VCC to Relative GND[1] ... –0.5V to +4.6V
DC Voltage Applied to Outputs in High Z State[1] .................... –0.5V to VCC + 0.5V
DC Input Voltage[1] ............................................ –0.5V to VCC + 0.5V

Electrical Characteristics Over the Operating Range

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>7C1019CV33 -8</th>
<th>7C1019CV33 -10</th>
<th>7C1019CV33 -12</th>
<th>7C1019CV33 -15</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOH</td>
<td>Output HIGH Voltage</td>
<td>VCC = Min., IOH = –4.0 mA</td>
<td>2.4</td>
<td>2.4</td>
<td>2.4</td>
<td>2.4</td>
</tr>
<tr>
<td>VOL</td>
<td>Output LOW Voltage</td>
<td>VCC = Min., IOL = 8.0 mA</td>
<td>0.4</td>
<td>0.4</td>
<td>0.4</td>
<td>0.4</td>
</tr>
<tr>
<td>VIH</td>
<td>Input HIGH Voltage</td>
<td>2.0 VCC + 0.3</td>
<td>2.0 VCC + 0.3</td>
<td>2.0 VCC + 0.3</td>
<td>2.0 VCC + 0.3</td>
<td>V</td>
</tr>
<tr>
<td>VIL[1]</td>
<td>Input LOW Voltage</td>
<td>–0.3</td>
<td>0.8</td>
<td>–0.3</td>
<td>0.8</td>
<td>–0.3</td>
</tr>
<tr>
<td>IIX</td>
<td>Input Load Current</td>
<td>GND ≤ VIX ≤ VCC</td>
<td>–1</td>
<td>+1</td>
<td>–1</td>
<td>+1</td>
</tr>
<tr>
<td>IOZ</td>
<td>Output Leakage Current</td>
<td>GND ≤ VIZ ≤ VCC, Output Disabled</td>
<td>–1</td>
<td>+1</td>
<td>–1</td>
<td>+1</td>
</tr>
<tr>
<td>IOS[2]</td>
<td>Output Short Circuit Current</td>
<td>VCC = Max., VOUT = GND</td>
<td>–300</td>
<td>–300</td>
<td>–300</td>
<td>–300</td>
</tr>
<tr>
<td>ICC</td>
<td>VCC Operating Supply Current</td>
<td>VCC = Max., IOUT = 0 mA, f = fMAX = 1/RC</td>
<td>85</td>
<td>80</td>
<td>75</td>
<td>70</td>
</tr>
<tr>
<td>ISB1</td>
<td>Automatic CE Power-down Current —TTL Inputs</td>
<td>Max. VCC, CE ≥ VIH</td>
<td>15</td>
<td>15</td>
<td>15</td>
<td>15</td>
</tr>
<tr>
<td>ISB2</td>
<td>Automatic CE Power-down Current —CMOS Inputs</td>
<td>Max. VCC, CE ≥ VCC – 0.3V, or VCC – 0.3V, or VCC ≤ 0.3V, f = 0</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>5</td>
</tr>
</tbody>
</table>

Capacitance[3]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Test Conditions</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>CIN</td>
<td>Input Capacitance</td>
<td>T A = 25°C, f = 1 MHz, VCC = 5.0V</td>
<td>8</td>
<td>pF</td>
</tr>
<tr>
<td>COUT</td>
<td>Output Capacitance</td>
<td></td>
<td>8</td>
<td>pF</td>
</tr>
</tbody>
</table>

Notes:
1. VIL (min.) = –2.0V for pulse durations of less than 20 ns.
2. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
3. Tested initially and after any design or process changes that may affect these parameters.
AC Test Loads and Waveforms\[4\]

**8-ns devices:**

\[\text{OUTPUT} \xrightarrow{Z=50\Omega} 50\Omega \xrightarrow{1.5V} 30pF* \]

* CAPACITIVE LOAD CONSISTS OF ALL COMPONENTS OF THE TEST ENVIRONMENT

(a)

**10-, 12-, 15-ns devices:**

\[\text{OUTPUT} \xrightarrow{3.3V} 30pF \xrightarrow{R 317\Omega} R2 \xrightarrow{351\Omega} 50\Omega \xrightarrow{1.5V} 30pF* \]

(b)

**High-Z characteristics:**

\[\text{OUTPUT} \xrightarrow{3.3V} 5pF \xrightarrow{R 317\Omega} R2 \xrightarrow{351\Omega} \]

(d)

**Notes:**

4. AC characteristics (except High-Z) for all 8ns parts are tested using the load conditions shown in Figure (a). All other speeds are tested using the Thevenin load shown in Figure (b). High-Z characteristics are tested for all speeds using the test load shown in Figure (d).
## Switching Characteristics Over the Operating Range

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>7C1019CV33-8</th>
<th>7C1019CV33-10</th>
<th>7C1019CV33-12</th>
<th>7C1019CV33-15</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Read Cycle</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tRC</td>
<td>Read Cycle Time</td>
<td>8</td>
<td>10</td>
<td>12</td>
<td>15</td>
</tr>
<tr>
<td>tAA</td>
<td>Address to Data Valid</td>
<td>8</td>
<td>10</td>
<td>12</td>
<td>15</td>
</tr>
<tr>
<td>tOHA</td>
<td>Data Hold from Address Change</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>tACE</td>
<td>CE LOW to Data Valid</td>
<td>8</td>
<td>10</td>
<td>12</td>
<td>15</td>
</tr>
<tr>
<td>tDOE</td>
<td>OE LOW to Data Valid</td>
<td>5</td>
<td>5</td>
<td>6</td>
<td>7</td>
</tr>
<tr>
<td>tLZCE</td>
<td>OE LOW to Low Z</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>tHZOE</td>
<td>OE HIGH to High Z[^6, 7]</td>
<td>4</td>
<td>5</td>
<td>6</td>
<td>7</td>
</tr>
<tr>
<td>tLZCE</td>
<td>CE LOW to Low Z[^6]</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>tHZCE</td>
<td>CE HIGH to High Z[^6, 7]</td>
<td>4</td>
<td>5</td>
<td>6</td>
<td>7</td>
</tr>
<tr>
<td>tPU[^8]</td>
<td>CE LOW to Power-Up</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>tPD[^8]</td>
<td>CE HIGH to Power-Down</td>
<td>8</td>
<td>10</td>
<td>12</td>
<td>15</td>
</tr>
<tr>
<td><strong>Write Cycle</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tWC</td>
<td>Write Cycle Time</td>
<td>8</td>
<td>10</td>
<td>12</td>
<td>15</td>
</tr>
<tr>
<td>tSCE</td>
<td>CE LOW to Write End</td>
<td>7</td>
<td>8</td>
<td>9</td>
<td>10</td>
</tr>
<tr>
<td>tAW</td>
<td>Address Set-Up to Write End</td>
<td>7</td>
<td>8</td>
<td>9</td>
<td>10</td>
</tr>
<tr>
<td>tSA</td>
<td>Address Hold from Write End</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>tSA</td>
<td>Address Set-Up to Write Start</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>tPWE</td>
<td>WE Pulse Width</td>
<td>6</td>
<td>7</td>
<td>8</td>
<td>10</td>
</tr>
<tr>
<td>tSD</td>
<td>Data Set-Up to Write End</td>
<td>5</td>
<td>5</td>
<td>6</td>
<td>8</td>
</tr>
<tr>
<td>tHD</td>
<td>Data Hold from Write End</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>tLZWE</td>
<td>WE HIGH to Low Z[^7]</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>tHZWE</td>
<td>WE LOW to High Z[^6, 7]</td>
<td>4</td>
<td>5</td>
<td>6</td>
<td>7</td>
</tr>
</tbody>
</table>

Notes:

5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.
6. tLZCE, tLZOE, and tLZWE are specified with a load capacitance of 5 pF as in part (d) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
7. At any given temperature and voltage condition, tHZCE is less than tLZCE, tHZOE is less than tLZOE, and tHZWE is less than tLZWE for any given device.
8. This parameter is guaranteed by design and is not tested.
9. The internal write time of the memory is defined by the overlap of CE LOW and WE LOW. CE and WE must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
10. The minimum write cycle time for Write Cycle no. 3 (WE controlled, OE LOW) is the sum of tLZWE and tSD.
Switching Waveforms

Read Cycle No. 1\[11, 12]\n
Read Cycle No. 2 (OE Controlled)\[12, 13]\n
Write Cycle No. 1 (CE Controlled)\[14, 15]\n
Notes:
11. Device is continuously selected. OE, CE = VIL.
12. WE is HIGH for read cycle.
13. Address valid prior to or coincident with CE transition LOW.
14. Data I/O is high impedance if OE = VIL.
15. If CE goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.
Switching Waveforms (continued)

Write Cycle No. 2 (WE Controlled, OE HIGH During Write)\textsuperscript{[14, 15]}

Write Cycle No. 3 (WE Controlled, OE LOW)\textsuperscript{[15]}

\textbf{Note:}
16. During this period the I/Os are in the output state and input signals should not be applied.
### Truth Table

<table>
<thead>
<tr>
<th>CE</th>
<th>OE</th>
<th>WE</th>
<th>I/O0—I/O7</th>
<th>Mode</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>X</td>
<td>X</td>
<td>High Z</td>
<td>Power-Down</td>
<td>Standby (I(SB))</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>High Z</td>
<td>Power-Down</td>
<td>Standby (I(SB))</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
<td>Data Out</td>
<td>Read</td>
<td>Active (I(CC))</td>
</tr>
<tr>
<td>L</td>
<td>X</td>
<td>L</td>
<td>Data In</td>
<td>Write</td>
<td>Active (I(CC))</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>H</td>
<td>High Z</td>
<td>Selected, Outputs Disabled</td>
<td>Active (I(CC))</td>
</tr>
</tbody>
</table>

### Ordering Information

<table>
<thead>
<tr>
<th>Speed (ns)</th>
<th>Ordering Code</th>
<th>Package Name</th>
<th>Package Type</th>
<th>Operating Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>CY7C1019CV33-8VC</td>
<td>V33</td>
<td>32-Lead 400-Mil Molded SOJ</td>
<td>Commercial</td>
</tr>
<tr>
<td></td>
<td>CY7C1019CV33-8VI</td>
<td>V33</td>
<td>32-Lead 400-Mil Molded SOJ</td>
<td>Industrial</td>
</tr>
<tr>
<td>10</td>
<td>CY7C1019CV33-10VC</td>
<td>V33</td>
<td>32-Lead 400-Mil Molded SOJ</td>
<td>Commercial</td>
</tr>
<tr>
<td></td>
<td>CY7C1019CV33-10ZC</td>
<td>ZS32</td>
<td>32-Lead TSOP II</td>
<td>Industrial</td>
</tr>
<tr>
<td></td>
<td>CY7C1019CV33-10VI</td>
<td>V33</td>
<td>32-Lead 400-Mil Molded SOJ</td>
<td>Commercial</td>
</tr>
<tr>
<td></td>
<td>CY7C1019CV33-10ZI</td>
<td>ZS32</td>
<td>32-Lead TSOP II</td>
<td>Industrial</td>
</tr>
<tr>
<td>12</td>
<td>CY7C1019CV33-12VC</td>
<td>V33</td>
<td>32-Lead 400-Mil Molded SOJ</td>
<td>Commercial</td>
</tr>
<tr>
<td></td>
<td>CY7C1019CV33-12ZC</td>
<td>ZS32</td>
<td>32-Lead TSOP II</td>
<td>Industrial</td>
</tr>
<tr>
<td></td>
<td>CY7C1019CV33-12VI</td>
<td>V33</td>
<td>32-Lead 400-Mil Molded SOJ</td>
<td>Commercial</td>
</tr>
<tr>
<td></td>
<td>CY7C1019CV33-12ZI</td>
<td>ZS32</td>
<td>32-Lead TSOP II</td>
<td>Industrial</td>
</tr>
<tr>
<td>15</td>
<td>CY7C1019CV33-15VC</td>
<td>V33</td>
<td>32-Lead 400-Mil Molded SOJ</td>
<td>Commercial</td>
</tr>
<tr>
<td></td>
<td>CY7C1019CV33-15ZC</td>
<td>ZS32</td>
<td>32-Lead TSOP II</td>
<td>Industrial</td>
</tr>
<tr>
<td></td>
<td>CY7C1019CV33-15VI</td>
<td>V33</td>
<td>32-Lead 400-Mil Molded SOJ</td>
<td>Commercial</td>
</tr>
<tr>
<td></td>
<td>CY7C1019CV33-15ZI</td>
<td>ZS32</td>
<td>32-Lead TSOP II</td>
<td>Industrial</td>
</tr>
</tbody>
</table>
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<table>
<thead>
<tr>
<th>REV.</th>
<th>ECN NO.</th>
<th>Issue Date</th>
<th>Orig. of Change</th>
<th>Description of Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>**</td>
<td>109245</td>
<td>12/16/01</td>
<td>HGK</td>
<td>New Data Sheet</td>
</tr>
<tr>
<td>*A</td>
<td>113431</td>
<td>04/10/02</td>
<td>NSL</td>
<td>AC Test Loads split based on speed</td>
</tr>
<tr>
<td>*B</td>
<td>115047</td>
<td>08/01/02</td>
<td>HGK</td>
<td>Added TSOP II Package and Temp. Improved $I_{CC}$ limits</td>
</tr>
</tbody>
</table>