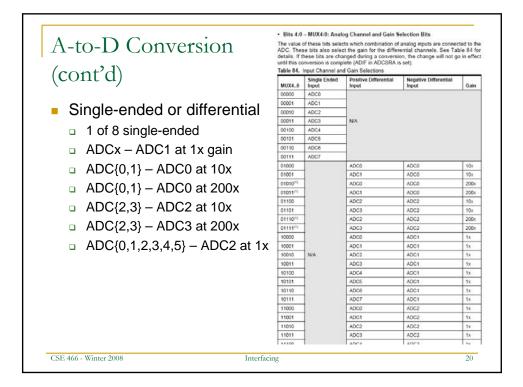
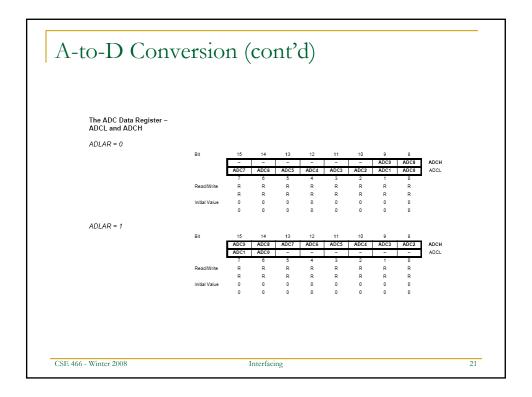
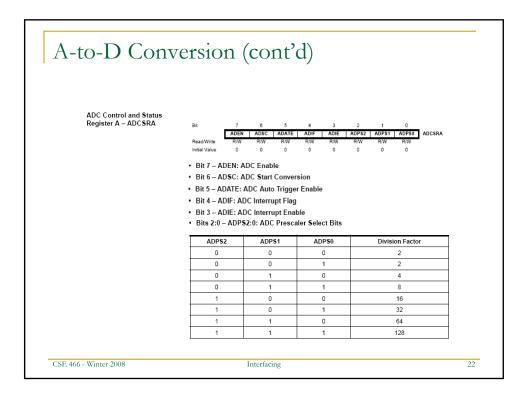


ADC Multiplexer Selection Register – ADMUX	Bit 7 6 5 4 3 2 1 0 ReadWrite Initial Value 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0			
	Table 83. Voltage Reference Selections for ADC REFS1 REFS0 Voltage Reference Selection			
	0 0 AREF. Internal Viet turned off			
	0 1 AVCC with external capacitor at AREF pin			
	1 0 Reserved			
	1 1 Internal 2.56V Voltage Reference with external capacitor at AREF			
	 Bit 5 – ADLAR: ADC Left Adjust Result The ADLAR bit affects the presentation of the ADC conversion result in the ADC Data Register. Write one to ADLAR to left adjust the result. Otherwise, the result is righ adjusted. Chanarian the ADLAR bit will affect the ADC Data Recister immediately regardless of any ongoing conversions. For a complete description of this bit, see "The ADC Data Register – ADCL and ADCH" on page 218. 			







				,		
Special FunctionIO Register SFIOR						
SHOK	Bit	7 6 ADTS2 ADTS1	5 ADTS0	4 3 2 1 D - ACME PUD PSR2 PSR10 SFIOR		
	Read/Write	R/W R/W	R/W	R R/W R/W R/W R/W		
	Initial Value	0 0	0	0 0 0 0 0		
	• Bit 7:5 – A	Bit 7:5 – ADT\$2:0: ADC Auto Trigger Source				
	trigger an ADC conversion. If ADATE is cleared, the ADTS2.0 settings will have no effect. A conversion will be triggered by the rising edge of the selected Interrupt Flag. Note that switching from a trigger source that is cleared to a trigger source that is set, will generate a positive edge on the trigger signal. If ADEN in ADCSRA is set, this will start a conversion. Switching to Free Running mode (ADTS[2:0]=0) will not cause a trig- ger event, even if the ADC Interrupt Flag is set. Table 86. ADC Auto Trigger Source Selections					
	ADTS2	ADTS1	ADTS0	Trigger Source		
	0	0	0	Free Running mode		
	0	0	1	Analog Comparator		
	0	1	0	External Interrupt Request 0		
	0	1	1	Timer/Counter0 Compare Match		
		0	0	Timer/Counter0 Overflow		
	1					
	1	0	1	Timer/Counter Compare Match B		
		0	1	Timer/Counter Compare Match B Timer/Counter1 Overflow		
	1	-				

