YAMAHA

YMU757B

MA-1C

Outline

The YMU757B is a high quality melody LSI for cellular phone handsets, supporting the data format for various applications including ringing and holding melody sounds. The built-in Yamaha's original FM synthesizer can create various timbres, and its built-in sequencer can produce up to 4 different sounds with 4 different timbres simultaneously without placing a load to the controller.

The serial port controller interface enables real time reproduction of the melody data via FIFO, without the limitation of the data capacity.

With a built-in amplifier to drive the dynamic type speaker, it is possible to connect the speaker directly.

This LSI also has an analog-output terminal for the phone jack. In the stand-by mode, the power consumption can be reduced to 1 μA or less while waiting.

Features

- YAMAHA's original FM sound generator function
- Built-in sequencer
- Capable of producing up to 4 different sounds simultaneously (4 independent timbres available).
- Built-in output 400mW speaker amplifier
- Built-in circuit for sound quality correcting equalizer
- Built-in serial interface
- 2.688, 8.4, 12.6, 14.4, 19.2, 19.68, 19.8 and 27.82 MHz serial clock inputs support
  And support the mode which set to optional frequency from 2.685MHz to 27.853MHz at 55.93kHz intervals
- Analog output for ear phone
- Power down mode (Typ 1μA or less)
- Power supply voltage (Digital and Analog): 3.0V±10 %
- 20-pin QFN
  The plating of pins is lead-free. (YMU757B-QZ)

YAMAHA CORPORATION

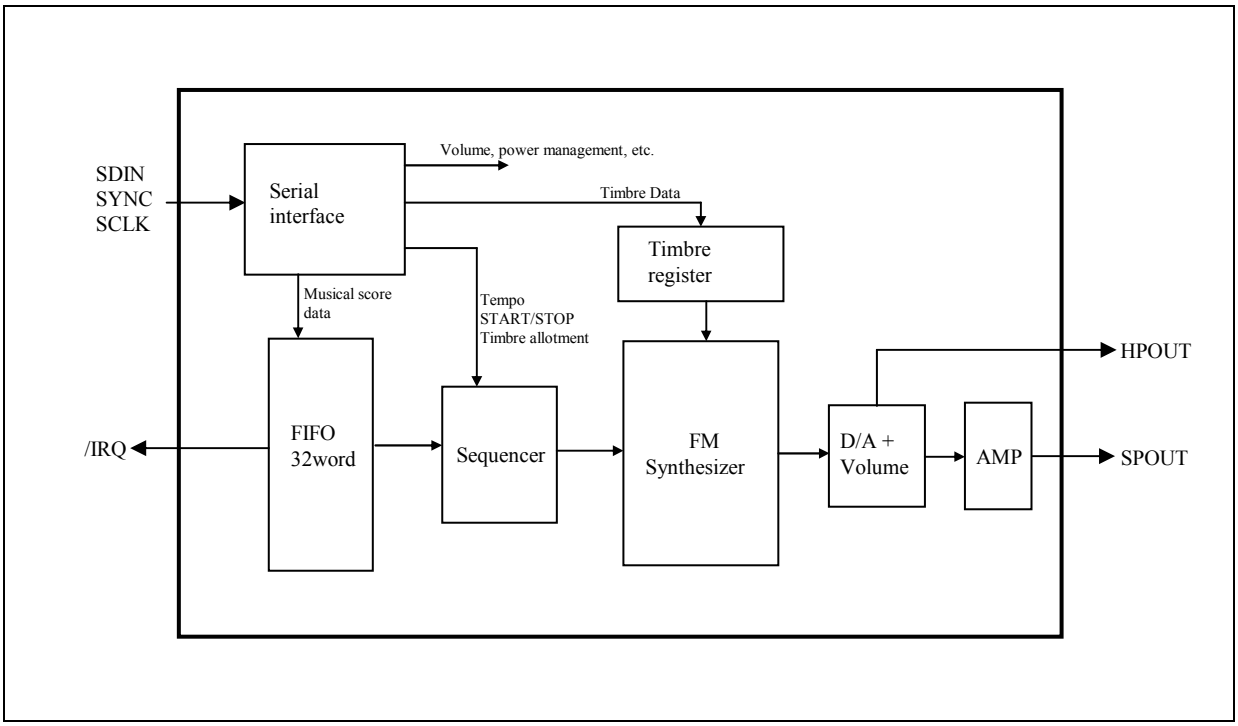
YMU757B CATALOG
CATALOG No.:LSI-4MU757B3
2004.4

Contents

■General description of YMU757B

The YMU757B is controlled by way of the serial interface.

Shown below is its internal configuration.



When the data is inputted into the serial interface, it is converted into the parallel data and transmitted to each function block according to the index address.

The musical score data is stored in the 32-word FIFO first and then transmitted to the sequencer where it is interpreted and signals to control sound generation of the FM synthesizer is output.

The timbre register is where up to 8 timber data can be stored.

Also, as the sequencer controlling parameters, the start/stop and tempo signals are provided.

In order to have sound generated, the following processes must be performed for this LSI.

1) Initial status setting (cancellation of power-down function, clock selection, etc.)
2) Timbre data setting
3) Writing the musical score data in FIFO before starting the sequence
4) Writing the next musical score data before FIFO becomes empty upon receipt of the interrupt signal from FIFO during reproduction,.

(For the details, refer to "Settings and procedure to generate melody".)

Block description

1) Serial interface

When the serial interface receives the serial data, it identifies the index data and transmits the control data to each function block.

2) FIFO

The musical score data are stored temporarily in FIFO which can contain up to 32 musical score data. The musical score data are processed are processed in the sequencer when they are generated as sounds and those that have been processed are deleted one after another. When the remaining data amount in FIFO reaches the register setting (IRQ point) or less, it outputs an interrupt signal to ask for the continuing musical score data to be fed.

3) Sequencer

When the sequencer receives the START command, it starts to read the musical score data which have been stored in FIFO. The processed musical score data are deleted.

4) Timbre register (Index 10h~2Fh)

The timbre data are stored in this register which can contain up to 8 timbres. Settings for this register must be made before sound generation. Though it is initialized by hardware resetting, contents of a register aren't cleared, and the value which had light last time is held as for the following.

- Software reset (CLR bit of Index32h)
- After the inside of the power going down mode and a release.

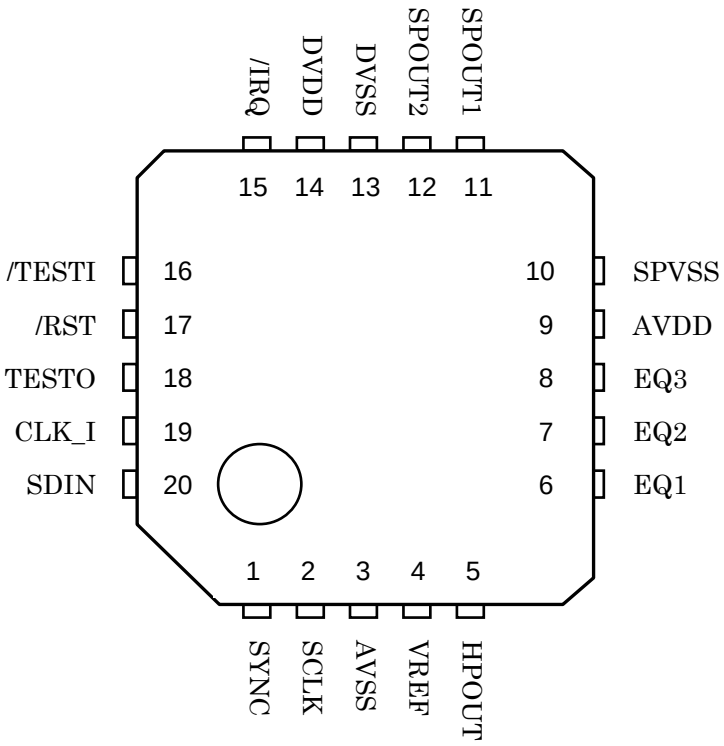
5) FM synthesizer

The timbres are synthesized and generated according to settings. Four sounds can be generated at the same time.

6) D/A, volume and amplifier

The outputs from the synthesizer are D/A converted and volume processed. After that, they are output from the speaker or the earphone out terminal.

■ Pin configuration



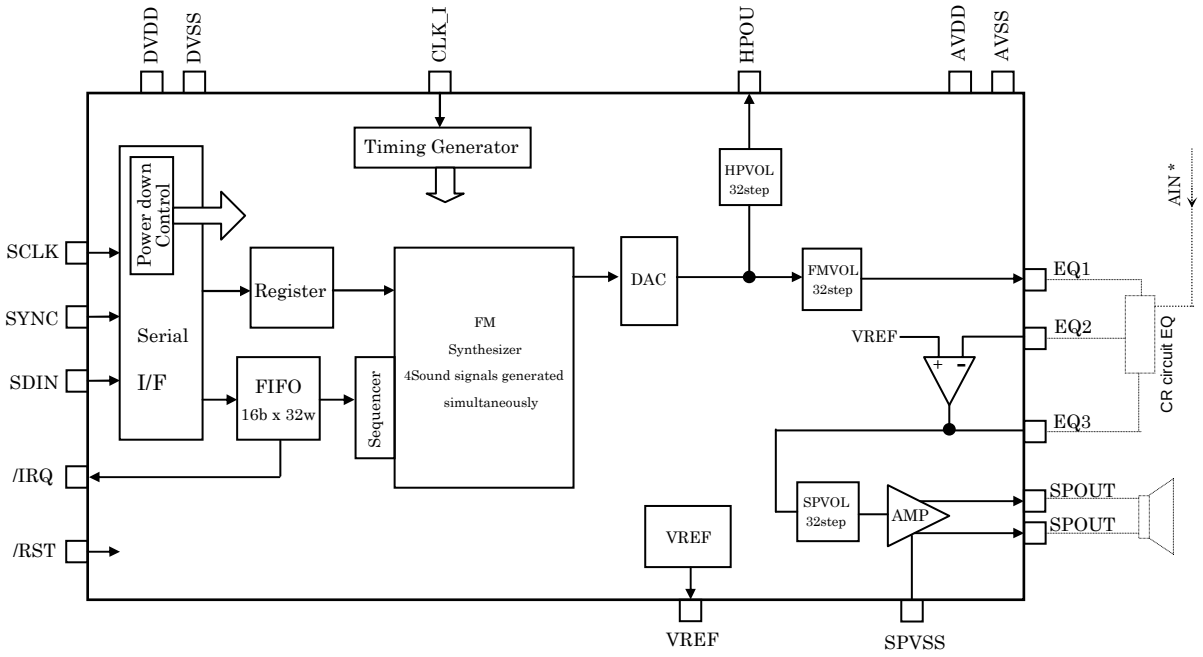
20 Pin QFN Top View

■ Pin description

No.	Pin	I/O	Function
1	SYNC	I	Serial I/F synchronous signal input
2	SCLK	Ish	Serial I/F bit clock input
3	AVSS	-	Analog ground
4	VREF	A	Analog reference voltage terminal Connect 0.1µF capacitor between this terminal and the analog ground terminal.
5	HPOUT	AO	Analog output terminal for ear phone
6	EQ1	AO	Equalizer terminal 1
7	EQ2	AI	Equalizer terminal 2
8	EQ3	AO	Equalizer terminal 3
9	AVDD	-	Analog power supply (+3.0V) Connect 0.1µF and 4.7µF capacitors between this terminal and the analog ground terminal
10	SPVSS	-	Analog ground exclusively used for speaker
11	SPOUT1	AO	Speaker output terminal 1
12	SPOUT2	AO	Speaker output terminal 2
13	DVSS	-	Digital ground
14	DVDD	-	Digital power supply (+3.0V) Connect 0.1µF and 4.7µF capacitors between this terminal and the digital ground terminal.
15	/IRQ	O	Interrupt signal output
16	/TESTI	I	LSI test input terminal (Always connect with DVDD.)
17	/RST	I	Hardware reset terminal
18	TESTO	O	LSI TEST output terminal (disconnected)
19	CLK_I	Ish	Clock input terminal
20	SDIN	I	Serial I/F data input

Note : Ish = Schmitt input terminal AI = Analog input terminal A0 = Analog output terminal

Block diagram



Concerning AIN signal inputted into equalizer circuit
As this design presupposes the use of this LSI for the "hands-free", it is possible to process the FM sound and call sound by analog mixing in the equalizer circuit and output the resulting sound through the speaker.

■ Register map

Index	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0	Description
$00h	BL1	BL0	NT3	NT2	NT1	NT0	CH1	CH0	VIB	TI3	TI2	TI1	TI0	TK2	TK1	TK0	Note data
	0	0	1	1	0	0	CH1	CH0	VCHE	TI3	TI2	TI1	TI0	VCH2	VCH1	VCH0	Rest data
$10 - 2Fh	ML2	ML1	ML0	VIB	EGT	SUS	RR3	RR2	RR1	RR0	DR3	DR2	DR1	DR0	AR3	AR2	Timbre data (Left data
	AR1	AR0	SL3	SL2	SL1	SL0	TL5	TL4	TL3	TL2	TL1	TL0	WAV	FL2	FL1	FL0	for 1 timbre)
$30h	0	V32	V31	V30	0	V22	V21	V20	0	V12	V11	V10	0	V02	V01	V00	Timbre allotment data
$31h	0	0	0	0	0	0	0	0	T7	T6	T5	T4	T3	T2	T1	T0	Tempo data
$32h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CLR	ST	FM Control
$33h	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKSEL			CLK_I select
$34h	0	0	0	0	0	0	0	0	0	0	IRQE	IRQ Point					IRQ Control
$35h	0	0	0	0	0	0	0	0	0	0	0	V4	V3	V2	V1	V0	Speaker Volume
$36h	0	0	0	0	0	0	0	0	0	0	0	V4	V3	V2	V1	V0	FM Volume
$37h	0	0	0	0	0	0	0	0	0	0	0	V4	V3	V2	V1	V0	HPOUT Volume
$38h	0	0	0	0	0	0	0	0	0	0	0	AP4	AP3	AP2	AP1	DP	Power Management
$39h	0	0	0	0	0	0	0	CLKSET									CLK_I Select
$40 - EFh	Reserved (access prohibited)																Reserved
$F0 - FFh	For LSI TEST(access prohibited)																LSI TEST

Note : Making an access to the spaces marked "Reserved" and "For LSI TEST" in the above table is prohibited.

Be sure to write "0" for the empty bit, although writing "1" there will not affect the LSI operation.

■ Explanation of registers

The YMU757B has three types of control registers. They are musical score data, timbre data and other control data.

□ Musical score data

$00h Musical score data

The musical score data are written in FIFO whose capacity is 32 words. There are two types of musical score data; note data and rest data.

Note data Default: 0000h

Index	B15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
$00h	BL1	BL0	NT3	NT2	NT1	NT0	CH1	CH0	VIB	TI3	TI2	TI1	TI0	TK2	TK1	TK0

BL1 – BL0 : Octave block setting

Three octave blocks are available for sound range setting. The setting range is 1 to 3. Do not use "0" for setting.

The sound generation range involves the coefficient named "Multiple (multiplying factor for sound frequency).

By combining the octave block and Multiple settings, sounds can be generated in the ranges as listed in the table blow.

Since the setting ranges of "Multiple" coefficient is 0 to 7, actually, sounds can be generated in a wider ranges than those given in the table below.

	Multiple = 1 (x1)	Multiple = 2 (x2)	Multiple = 4 (x4)
BL[1:0] = 01b	C#3 (139Hz)	C#4 (277Hz)	C#5 (554Hz)
	D3 (147Hz)	D4 (294Hz)	D5 (587Hz)
	D#3 (156Hz)	D#4 (311Hz)	D#5 (622Hz)
	E3 (165Hz)	E4 (330Hz)	E5 (659Hz)
	F3 (175Hz)	F4 (349Hz)	F5 (698Hz)
	F#3 (185Hz)	F#4 (370Hz)	F#5 (740Hz)
	G3 (196Hz)	G4 (392Hz)	G5 (784Hz)
	G#3 (208Hz)	G#4 (415Hz)	G#5 (831Hz)
	A3 (220Hz)	A4 (440Hz)	A5 (880Hz)
	A#3 (233Hz)	A#4 (466Hz)	A#5 (932Hz)
	B3 (247Hz)	B4 (494Hz)	B5 (988Hz)
	C4 (262Hz)	C5 (523Hz)	C6 (1046Hz)
BL[1:0] = 10b	C#4 (277Hz)	C#5 (554Hz)	C#6 (1109Hz)
	D4 (294Hz)	D5 (587Hz)	D6 (1175Hz)
	D#4 (311Hz)	D#5 (622Hz)	D#6 (1245Hz)
	E4 (330Hz)	E5 (659Hz)	E6 (1319Hz)
	F4 (349Hz)	F5 (698Hz)	F6 (1397Hz)
	F#4 (370Hz)	F#5 (740Hz)	F#6 (1480Hz)
	G4 (392Hz)	G5 (784Hz)	G6 (1568Hz)
	G#4 (415Hz)	G#5 (831Hz)	G#6 (1661Hz)
	A4 (440Hz)	A5 (880Hz)	A6 (1760Hz)
	A#4 (466Hz)	A#5 (932Hz)	A#6 (1865Hz)
	B4 (494Hz)	B5 (988Hz)	B6 (1976Hz)
	C5 (523Hz)	C6 (1046Hz)	C7 (2093Hz)
BL[1:0] = 11b	C#5 (554Hz)	C#6 (1109Hz)	C#7 (2217Hz)
	D5 (587Hz)	D6 (1175Hz)	D7 (2349Hz)
	D#5 (622Hz)	D#6 (1245Hz)	D#7 (2489Hz)
	E5 (659Hz)	E6 (1319Hz)	E7 (2637Hz)
	F5 (698Hz)	F6 (1397Hz)	F7 (2794Hz)
	F#5 (740Hz)	F#6 (1480Hz)	F#7 (2960Hz)
	G5 (784Hz)	G6 (1568Hz)	G7 (3136Hz)

	G#5 (831Hz)	G#6 (1661Hz)	G#7 (3322Hz)
	A5 (880Hz)	A6 (1760Hz)	A7 (3520Hz)
	A#5 (932Hz)	A#6 (1865Hz)	A#7 (3729Hz)
	B5 (988Hz)	B6 (1976Hz)	B7 (3951Hz)
	C6 (1046Hz)	C7 (2093Hz)	C8 (4186Hz)

NT3 - NT0 : Pitch setting

Four bits from NT3 to 0 are used to specify the pitch. The bit assignment is as shown below.

NT[3:0]	Pitch
0h	Prohibition
1h	C#
2h	D
3h	D#
4h	Prohibition
5h	E
6h	F
7h	F#
8h	Prohibition
9h	G
Ah	G#
Bh	A
Ch	Prohibition
Dh	A#
Eh	B
Fh	C

About "prohibition of a setup"

Though LSI never hangs up, different sound may be made. Never set it up.

CH1 - CH0 : Part setting

As the sound generator can generate sounds in 4 parts simultaneously, set the part for each note by using CH1 and 0 bits.

CH[1:0]	Part
00b	0
01b	1
10b	2
11b	3

VIB : Vibrato setting

This bit is used to set Vibrato function on or off for each note : "0" to set it off and "1" to set it on. The vibrato frequency is 6.4Hz and the modulation rate is ±13.47 cent.

When VIB bit of timbre data($10-2Fh) is "0", Vibrato function off.

TI3 - TI0 : Interval setting

These bits are used to set the interval period before the note and rest are processed next. The interval "48" represents the time for the whole note.

TI [3:0]	Interval
0h	0
1h	2
2h	3
3h	4
4h	6
5h	8
6h	9
7h	12
8h	18
9h	24
Ah	48
Bh	0
Ch	16
Dh	24
Eh	36
Fh	48

TK2 – TK0 : Note (sound length) designation

These 3 bits are used to designate the note (sound length). Depending on the values of interval setting (TI3 - 0), the length varies as shown in the following table. The interval "48" represents the time for the whole note.

	TI [3:0] = 0-Ah								TI [3:0] = B-Fh							
TK[2:0]	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
Sound length	1	2	3	5	7	8	11	17	15	23	29	32	35	41	47	Tie, Slur

Precaution

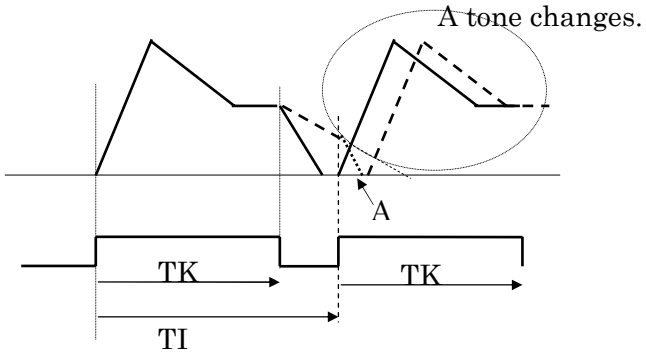
When KEY is turned on from the condition that a release rate isn't finished completely again in the same one channel, a tone may change.
This happens in the case of the continuous sound, even the decline sound which.
A reason happens because envelope of the career side of a source of FM sound and modulator side and a phase deviate.
The hardware creating the phase of a source of FM sound and envelope starts a movement by the following two conditions.

- A release rate is finished.
- Key ON occurs.

Tone data start a movement at the timing which modulator, a phase between the career, envelope are the same as. It is being based on what is done. When this condition isn't satisfied, a change in a tone occurs.

It explains by the following envelope figure.
It thinks that there is a tone which only release time is different from with the career and modulator as an example.
As for the condition that it stops completely, it moves to attack rate at the same time with KEY on.
If the last pronunciation is not the condition which stops completely while it is released, the setup of a release is made early forcibly, and it moves from the condition that (8.94mS) stops to attack rate.
(In the figure, the dotted line of A)

Though envelope of the solid line changes to attack rate soon at the time of second KEY ON, because sound of the dotted line doesn't stop completely, envelope can't move to attack rate soon.
It moves to attack rate after it becomes the condition that release time is made early and it stops completely. When both envelope and the start of the phase deviate and a tone varies according to the deviation of this time. Both envelope and the start of the phase deviate, and a tone changes by the deviation of this time.



How to avoid this symptom.
Try to pronounce it under the condition that a release stops completely.

Rest data Default: 0000h

Index	b15	b14	B13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
$00h	0	0	1	1	0	0	CH1	CH0	VCHE	TI3	TI2	TI1	TI0	VCH2	VCH1	VCH0

CH1 - CH0 : Part setting

Using CH1 or 0 bit, set the part for each rest.

CH[1:0]	Part
00b	0
01b	1
10b	2
11b	3

TI3 - TI0 : Interval setting

These bits are used to set the interval before the note and rest are processed next.

The interval "48" represents the time for the whole note.

The following table is exactly the same as that for the note data.

TI [3:0]	Interval
0h	3
1h	2
2h	3
3h	4
4h	6
5h	8
6h	9
7h	12
8h	18
9h	24
Ah	48
Bh	1
Ch	16
Dh	24
Eh	36
Fh	48

VCHE, VCH2 – VCH0 : Timbre change function

Although the maximum number of timbres that can be used simultaneously is four, the timbre can be changed during sound reproduction by setting these bits. Set "1" for VCHE and use VCH2 to VCH0 to set the timbre No.. Then starting with the note whose sound is to be generated next, the timbre for the part which has been set by using CH0 and 1 will be changed.

Change a tone after the pronunciation of a part to change stops completely.

The condition that pronunciation stops is not the condition that TK (pronunciation length) is finished, but the condition that the time when releases of envelope is finished.

Be careful because strange sound momentarily is pronounced when you change a tone under the condition that pronunciation doesn't stop completely.

If the timbre allotment is changed by using this function, the $30h register itself will be rewritten.

☐Timbre data

$10 – 2Fh Timbre data

It is possible to register the data for 8 timbres in the register and 4 among them can be reproduced simultane ously.

One timbre consists of [parameter for the modulator] and [parameter for the carrier] as a set.

(For the details of the modulator and the carrier, please refer to "General description of FM sound generator").

Index 10h, 11h …… Timbre data for the 1st timbre modulator
Index 12h, 13h …… Timbre data for the 1st timbre carrier
Index 14h, 15h …… Timbre data for the 2nd modulator
Index 16h, 17h …… Timbre data for the 2nd timbre carrier
…….Omitted…….
Index 2Ch, 2Dh …… Timbre data for the 8th timbre modulator
Index 2Eh, 2Fh …… Timbre data for the 8th timbre carrier

The following bit assignment is used for both modulator and carrier.
The setting must be completed before any sound is generated. It is prohibited to change the timbre parameter while any sound is generated.

Timbre data Default: 0000h

Index	B15	b14	b13	b12	B11	b10	B9	b8	b7	b6	b5	b4	b3	b2	b1	b0
EVEN	ML2	ML1	ML0	VIB	EGT	SUS	RR3	RR2	RR1	RR0	DR3	DR2	DR1	DR0	AR3	AR2
ODD	AR1	AR0	SL3	SL2	SL1	SL0	TL5	TL4	TL3	TL2	TL1	TL0	WAV	FL2	FL1	FL0

ML2 - ML0 : Multiple setting

"Multiple" refers to the multiplying factor for sound frequency. The output frequency is determined by the octave, pitch and multiple settings on the carrier side. On the modulator side, it is possible to adjust the multiple setting and create different timbres.

ML [2:0]	Multiplying factor for frequency
0h	x 1/2
1h	x 1
2h	x 2
3h	x 3
4h	x 4
5h	x 5
6h	x 6
7h	x 7

VIB : Vibrato

This function is used for setting the vibrato function on or off. Use "0" to set it off and "1" to set it on.

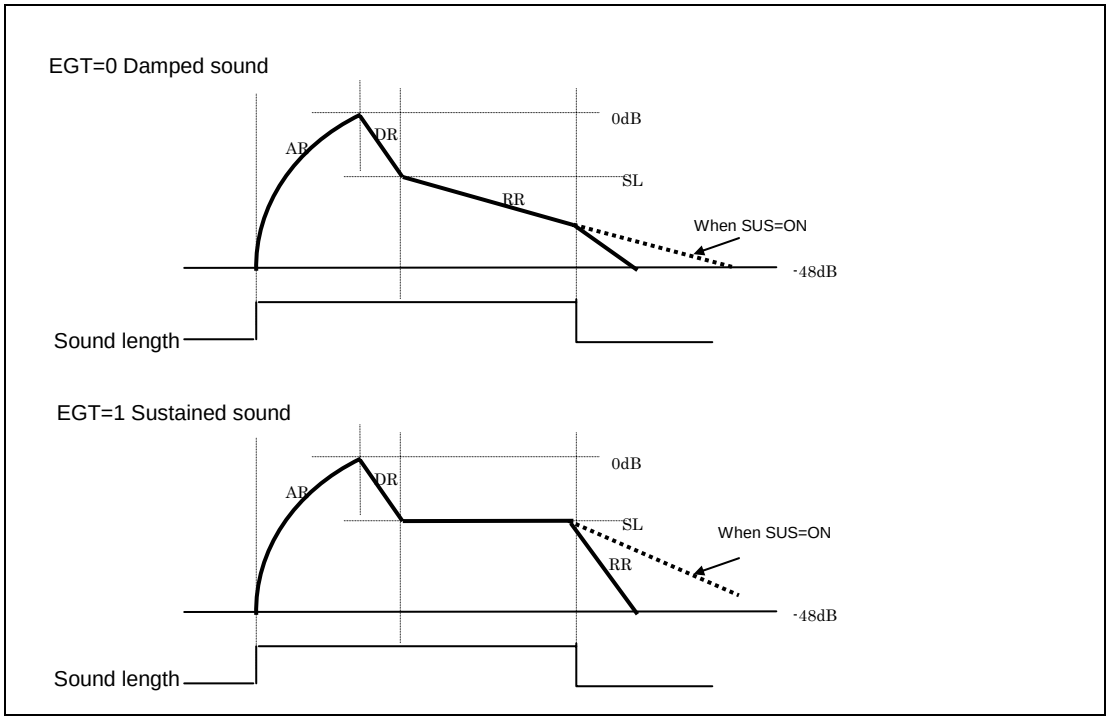
The vibrato frequency is 6.4Hz and the modulation rate is ±13.47cent.

EGT : Envelope waveform type

This function is used to select the type of the envelope waveform.

Use "0" for the damped sound and "1" for the sustained sound.

Shown below are the waveforms for the damped sound and sustained sound.



AR3 - AR0 : Attack rate setting

"Attack rate" refers to the time from start of the sound generation (-48dB) until it reaches the maximum volume (0dB).

The table on page 15 shows the settings by the time required to reach 0dB from –48dB.

DR3 - DR0 : Decay rate setting

The decay rate refers to the damping time required to reach the sustain level (SL) from the maximum volume level (0dB). The table below shows the settings by the time required to reach -48dB from 0dB.

RR3 - RR0 : Release rate setting

The release rate is defined differently for the damped sound and the sustained sound.

- In the case of the damped sound, it means the damping time from the sustain level to the end of the sound length. The sound is damped in 286ms (time to reach -48dB from 0dB) after the end of the sound length is reached.
- In the case of the sustained sound, it means the damping time from the end of the sound length.

SL3 - SL0 : Sustain level setting

The sustain level refers to the level at which shifting from the decay rate to the release rate takes place in the case of the damped sound, and the volume level of the sound being sustained in the case of the sustained sound.

SL ->	SL3	SL2	SL1	SL0
Weighted bit (dB)	-24	-12	-6	-3

AR[3:0] DR[3:0] RR[3:0]	Attack rate From -48 to 0dB (ms)	Decay rate, release rate from 0 to -48dB (ms)
Fh	0	2.23
Eh	4.65	8.94
Dh	9.30	17.88
Ch	18.59	35.76
Bh	37.19	71.52
Ah	74.38	143.04
9h	148.76	286.07
8h	297.51	572.14
7h	595.03	1144.25
6h	1190.05	2288.56
5h	2380.10	4577.12
4h	4760.21	9154.25
3h	9520.42	18308.50
2h	19040.84	36617.00
1h	∞	∞
0h	∞	∞

TL5 - TL0 : Total level setting

This function is used to set the envelope level.

TL	TL5	TL4	TL3	TL2	TL1	TL0
Weighted bit (dB)	-24	-12	-6	-3	-1.5	-0.75

SUS : Sustain On/OFF setting

"0" : OFF

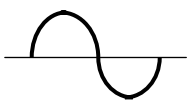
"1" : ON The release rate changes to "6" (2.29s) when the sound length comes to the end.

WAV : Waveform selection

The modulator and carrier can generate the SIN wave but when this bit setting is made, it is possible to generate a half-wave rectified waveform of the SIN wave, the timbres in wider range can be created.

"0" : SIN wave

"1" : Half-wave rectified waveform of the SIN wave.

WAV=0  WAV=1 

FL2 - FL0 : Feed-back setting

This function is effective for the operator on the carrier side only. It is used to set the feedback modulation rate.

Be sure to set "0" for the operator on the modulator side. This is effective when generating the strings.

FL [2:0]	0	1	2	3	4	5	6	7
Modulation rate	0	π/16	π/ 8	π/ 4	π/ 2	π	2π	4π

☐Other control data

$30h Timbre_allotment_data

One melody consists of four parts and a timbre is allotted for each of these parts. Among the eight timbres registered in the timbre data register, use four of them for each of these parts.

Default: 0000h

Index	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
$30h	0	V32	V31	V30	0	V22	V21	V20	0	V12	V11	V10	0	V02	V01	V00

"x" in Vx[2:0] means the part No.

The timbre data used with Vx[2:0] are as follows.

Vx[2:0]	Timbre data to be used
0h	Timbre set for index 10 to 13h is used.
1h	Timbre set for index 14 to 17h is used.
2h	Timbre set for index 18 to 1Bh is used.
3h	Timbre set for index 1C to 1Fh is used.
4h	Timbre set for index 20 to 23h is used.
5h	Timbre set for index 24 to 27h is used.
6h	Timbre set for index 28 to 2Bh is used.
7h	Timbre set for index 2C to 2Fh is used.

$31h Tempo_data

The "tempo" refers to the number of quarter notes reproduced in one minute. Use this setting to set the tempo of the melody used when reproduced. The setting data is (8739/TEMPO)-1

Default: 0000h

Index	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
$31h	0	0	0	0	0	0	0	0	T7	T6	T5	T4	T3	T2	T1	T0

$32h FM_section_control

Default: 0000h

Index	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
$32h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CLR	ST

ST : This bit is used to control start/stop of the melody. Use "1" for the start setting and "0" for the stop setting.

CLR : This bit is used to initialize the entire LSI by the software. All the one except for " Timbre data register" of Index10~2Fh are initialized. Bit CLR itself is not cleared when it is set as "1". Bit CLR should be written "0".

$33h Clock selection

Default: 0000h

Index	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
$33h	0	0	0	0	0	0	0	0	0	0	0	0	0	CLKSEL		

This setting sets the clock frequency inputted through the CLK_I terminal.

Be sure to execute this setting before reproducing the melody.

Even if clock of which frequency is being inputted during resetting, it is OK.

(As for the details of the establishment of clock, see on "about establishment of clock frequency".)

CKSEL [2:0]	Clock frequency (MHz)
0h(*)	2.688
1h	19.200
2h	19.680
3h	19.800
4h	8.400
5h	14.400
6h	27.821
7h	12.600

(*)When clock is set by programmable mode, set CLKSEL[2:0] to “0h”.

$34h Interrupt control

Default: 0000h

Index	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
$34h	0	0	0	0	0	0	0	0	0	0	IRQE	IRQ point				

The musical score data is taken into FIFO which has a capacity for 32 data. As the sounds are reproduced, the data in FIFO are processed and deleted. When the amount of data remaining in FIFO becomes less than the IRQ point set value, an interrupt signal is generated. At this point, set "0" for IRQE and write the continuing musical score data into FIFO. Make sure that the written data exceeds the IRQ point. After writing the data, reset "1" for IRQE and wait until another interrupt signal is generated.

IRQpoint can set 32 ways from 0 (empty) to 31 (1 data vacancy).

IRQE is enable bit. Set “1” for enable.

$35h Speaker volume control

$36h FM volume control

$37h Ear phone output volume control

Default: 0000h

Index	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
$35-7h	0	0	0	0	0	0	0	0	0	0	0	V4	V3	V2	V1	V0

These bits are used to set the volume of each source. The volume setting consists of 31 steps and mute function. It is possible to set at 1dB intervals. As the default is muted, cancel the mute function before proceeding to sound generation. Also, to reduce the power, be sure to mute the volume subject to power reduction before shifting.

Relations of register setting value and volume.

V[4:0]	Volume(dB)	V[4:0]	Volume(dB)	V[4:0]	Volume(dB)	V[4:0]	Volume(dB)
00h	MUTE	08h	-23	10h	-15	18h	-7
01h	-30	09h	-22	11h	-14	19h	-6
02h	-29	0Ah	-21	12h	-13	1Ah	-5
03h	-28	0Bh	-20	13h	-12	1Bh	-4
04h	-27	0Ch	-19	14h	-11	1Ch	-3
05h	-26	0Dh	-18	15h	-10	1Dh	-2
06h	-25	0Eh	-17	16h	- 9	1Eh	-1
07h	-24	0Fh	-16	17h	- 8	1Fh	0

$38h Power Management control

Default: 001Eh

Index	b15	b14	b13	b12	b11	B10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
$38h	0	0	0	0	0	0	0	0	0	0	0	AP4	AP3	AP2	AP1	DP

This setting is used to reduce the power of each function. It is possible to control 1 digital system and 4 analog systems independently. (For the details, please refer to "Power-down control division diagram".)
Setting all bits to "1" will minimize the power of the entire LSI.

DP : Use of "1" for this setting will reduce the power of the entire digital section.

AP1 : Use of "1" for this setting will reduce the power of the VREF circuit in the analog section.

AP2 : Use of "1" for this setting will reduce the power on the non-inverted amplifier side of the FM volume, speaker volume, equalizer circuit and speaker output section.

AP3 : Use of "1" for this setting will reduce the power of the inverted amplifier side of the speaker output section.

AP4 : Use of "1" for this setting will reduce the power of the DAC and ear phone output volume.

After initialization, the power of the analog section (AP1 to AP4) is reduced.

$39h Clock setting

Default: 0000h

Index	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
$39h	0	0	0	0	0	0	0	CLKSET								

When clock is set in programmable mode, the frequency of clock which it is inputted from the CLK_I terminal is set. Complete establishment before pronounce.

Even if clock of which frequency is being inputted during resetting, it is OK.

As for the details of the establishment of clock, which see "about establishment of clock frequency".

CLKSET [8:0]	Clock frequency(MHz)
000000000b	(Preset mode)
000000001b	Prohibition
:	:
000101111b	Prohibition
000110000b	2.684658000
000110001b	2.740588375
:	:
111110001b	27.797396375
111110010b	27.853326750
111110011b	Prohibition
:	:
111111111b	Prohibition

The value can be set to CLKSET are “000000000b", from "000110000b" to "111110010b".

If set value except for it, movement of LSI isn’t guaranteed.

Value to establish in CLKSET can be found by using the following ceremony.

CLKSET = Clock frequency [KHz] / 447.443 * 8

For example, when clock frequency is 3MHz, it becomes the following.

CLKSET = 3000 / 447.443 * 8 is about 54 = 000110110b

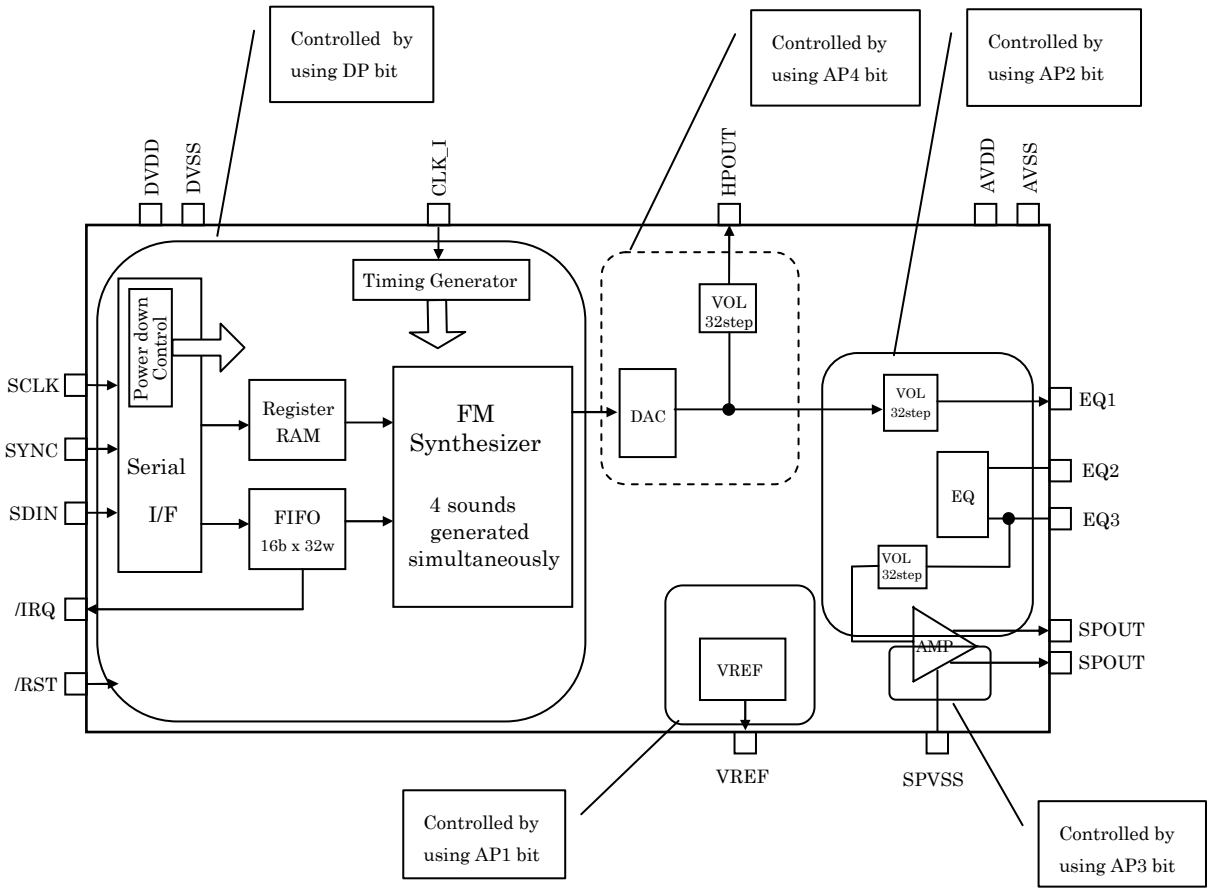
And, clock frequency is as follows.

Clock frequency [kHz] = 54 * 447.443 / 8 = 3020.24[kHz] = 3.02024[MHz]

Power-down control division diagram

As for the power-down, it is possible to divide an inside function separately and to control it.

The power-down is controlled by Index 38h.



Explanation of each bit

DP

It is the bit to make the power-down whole of the digital department.
Because clock to move inside stops consumption electric current of the digital part can be restrained in minimum.
Data on FIFO are cleared though contents of a register are held.

AP1

It is the bit that the power-down a VREF circuit decline.
If AP1 is set to “1”, the whole of the analog part stops. Because an analog center voltage is made by VREF circuit.

AP2

It is the bit to make power-down FM volume part, EQ circuit, speaker volume, and non-reversal amplifier side of speaker output part.

AP3

It is the bit that the power-down the reversal amplifier side of the speaker output part decline.
A reversal amplifier side is started after a VREF circuit and a non-reversal amplifier are started.
And, it depends, and pop noise occurrence can be restrained.

AP4

It is the bit that power-down DAC and the HP Volume part.

The attention point when the power-down moves.

Move from the condition that pronunciation surely stops for the power-down.
It is possible that the power-down a digital and an analog decline at the same time.
Be sure to mute FM Volume and HP Volume.
It is to restrain the noise when power going down.

The register which a digital part can't access during the power going down is as the following.

Index	Register functions
$00h	Note data
$10-2Fh	Tone data
$30h	Timbre allotment
$31h	Tempo data
$34h	IRQ Control

The attention point to cancel the power-down.

1 The time of 64×CLK_I is necessary before a digital part reverts to the normality after it is set up in DP=0.
Be sure to do register access after you wait for this time.

2 The following are procedure that revert from the condition in analog whole power-down and analog power supply off.

•AP1 is set to 0. VREF stands up at the time of maximum 50ms.
Until VREF stands up, don’t set “0” to AP2-AP4.
•AP2 is set to 0.
•AP3, AP4 are set to 0 after minimum 10μs.
•An analog part becomes possible it moves.
AP4 is set to 1 when used only a speaker amplifier part(hands free phone)
AP2,3 are set to 1 when a speaker amplifier isn't used and only head phone is used.
And it is possible that electric current is further restrained.

Analog power supply OFF mode

Only while pronunciation stops, it is possible that an analog power supply is turned off.
Turn off an analog power supply after AP1, AP2, AP3 and AP4 are set to 1.
It has the possibility that pop noise occurs if it doesn't do so.

The establishment example by the use case.

Depending on how the function is used, bit settings can be combined as shown below.

	AP1	AP2	AP3	AP4	Precaution
Power reduction of entire analog section	1	1	1	1	Be sure to set all volumes to "MUTE" first, then set all bits to "1" simultaneously.
Used for ear phone output only	0	1	1	0	Set the FM and speaker volumes to "MUTE".
Used for speaker only (hand-free phone)	0	0	0	1	Set the HP and FM volumes to "MUTE".

Resetting

This LSI can be initialized by setting the /RST terminal to "L" or through the software as the CLR bit is provided for the $32h setting.

The inside of the LSI is initialized by doing hardware resetting, and it becomes default condition.

It is completely initialized by software resetting except for the timbre data register of Index10h - 2Fh.

The FIFO data counter will be cleared and FIFO will be empty by initialize.

It is necessary to input CLK_I during resetting. Make sure to input CLK_I for at least 100 clocks during resetting.

After resetting is cancelled, wait for at least 64 clocks of CLK_I input and then start making an access to registers.

Settings and procedure to generate melody

Follow the steps as described below/

1. Set the CLKSEL ($33h) according to the clock frequency inputted for CLK_I.
2. Cancel the power-down mode of the analog section. (Refer to "Resetting sequence of analog section".)
3. Set the timbre data ($10-2Fh), timbre allotment data ($30h), tempo data ($31h) and volumes ($35-37h) as desired.
4. Enter 32 musical score data ($00h) until FIFO is full.
5. Set the IRQ point value of $34h. (Default at the center of FIFO).
6. Set "1" for IRQE of $34h
7. Set "1" for the ST bit of $32h and start the melody.

Setting of clock frequency

The establishment of clock frequency supports two forms of 'preset mode' and 'programmable mode'.

Preset mode: Select clock from 2.688 / 8.4 / 12.6 / 14.4 /19.2 / 19.68 / 19.8 / 27.82 MHz.

Programmable mode: Set to optional frequency from 2.685MHz to 27.853MHz at 55.93kHz intervals.

1)Using preset mode

The establishment of clock frequency can be done by establishing value in $33h with preset mode.

In this case, set “000000000b” to $39h. If set value except for it, movement of LSI isn’t guaranteed.

When value isn't established in either of $33h and $39h(default condition), becomes the condition that 2.688MHz is set with preset mode.

2)Using programmable mode

The establishment of clock frequency can be done by establishing value in $39h with programmable mode.

In this case, set “000b” to $33h. If set value except for it, movement of LSI isn’t guaranteed.

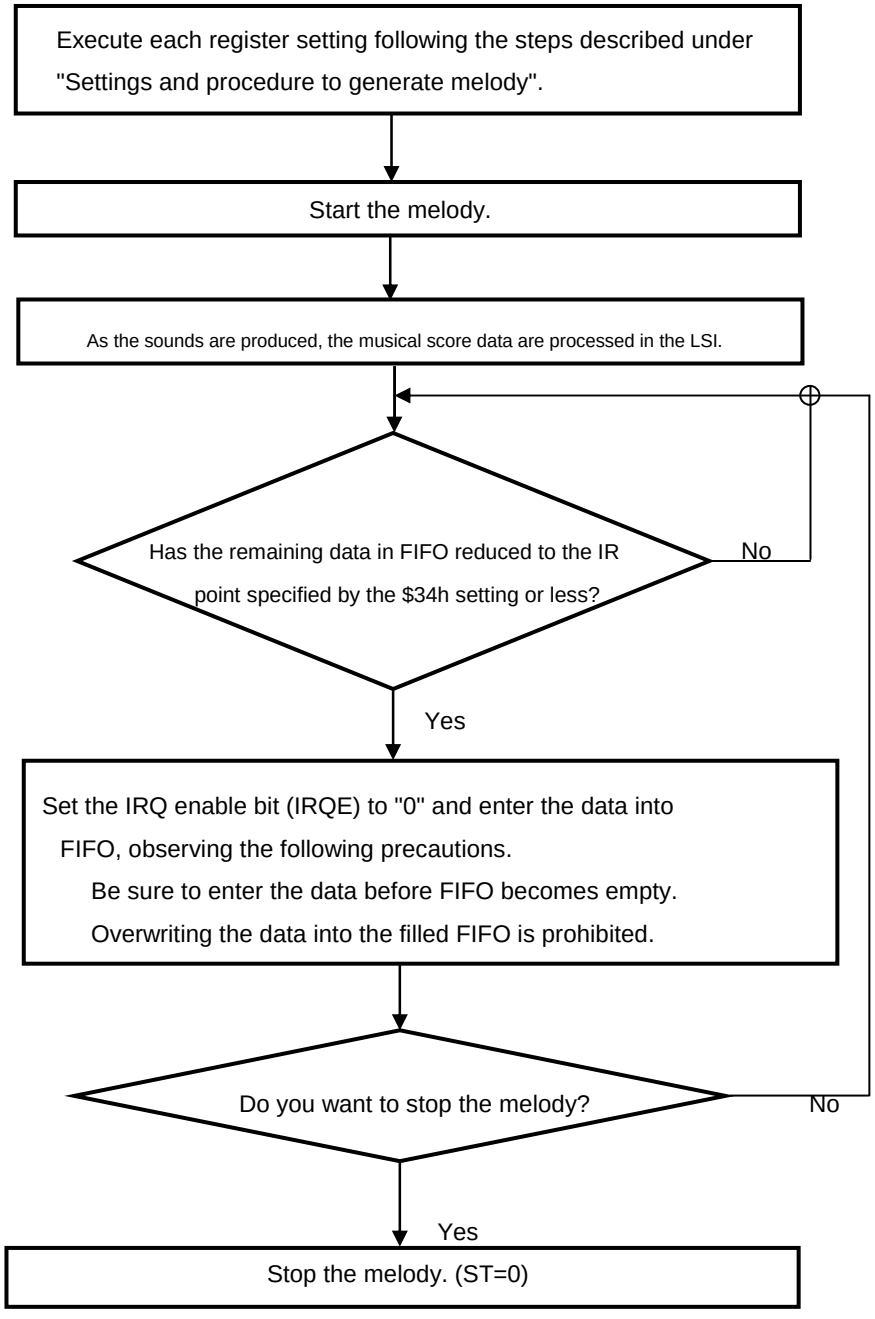
The value can be set to $39h are “000000000b", from "000110000b" to "111110010b".

If set value except for it, movement of LSI isn’t guaranteed.

Interrupt sequence

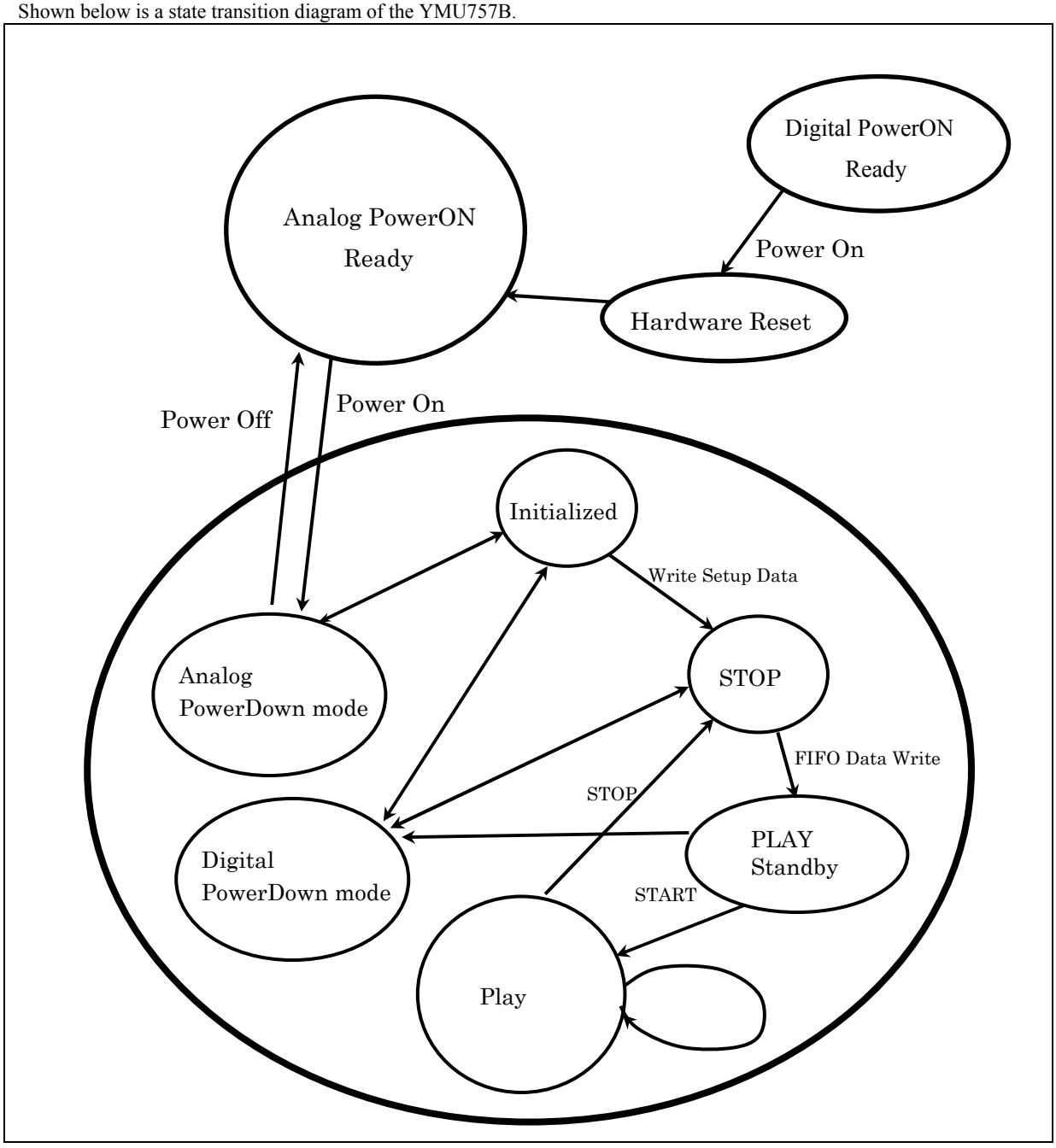
An interrupt from LSI (/IRQ-"L") occurs when the data amount in FIFO is less than the set value.
For example, supposing that 10h (16b) is set for the IRQ point of $34h, FIFO is full with the data before starting the melody as described above under "Settings and procedure to generate melody".
Once the melody is started, the musical score data is processed and the data in FIFO reduces continuously. When the remaining data amount becomes 16 bytes or less, the /IRQ terminal becomes "L" and an interrupt signal is transmitted to the external microprocessor.
When an interrupt signal is detected, set "0" for IRQE and enter the musical score data into FIFO before it becomes empty. As overwriting the data into the filled FIFO is prohibited, enter the data into FIFO by the amount not causing overwriting (16 data in this case).

Flow chart



State transition description

Shown below is a state transition diagram of the YMU757B.



Sequence to turn on the power supply.

Ideally, the digital side power supply should be turned on first to initialize the hardware, followed by turning on of the analog side power supply. If the analog power supply is turned on when the hardware has not been initialized, noises may be generated.

Explains about each status

Digital Power ON Ready

It is the condition before starting a digital power supply.

Hardware Reset

The digital power supply has been turned on. Immediately after it has turned on, always enter the hardware resetting data.

Analog Power ON Ready

It is the condition before starting a analog power supply. Turn on the analog power supply after the digital section has been initialized.

Analog Power Down mode

It is the state that the consumption electric power of the analog part is minimum.

After the analog power supply has been turned on, the entire analog section is in the power down state. In order to proceed to the next step Initialized state, use the procedure described on page 22. The power of the analog section has been reduced. The power consumption of the analog section can be reduced.

Be sure to take the procedure to reduce the power of the analog section from the initialized state. (That is, each volume must be set to "MUITE".)

It is possible to select the point where the power is reduced depending on the use purpose. For the details, refer to "Power-down sequence" on pages 21, 22 and 23.

To turn off the analog power supply, always take the necessary procedure from this state.

Initialized

Becomes this state when it comes out of the power down mode of the analog part, the digital part.

And, move to the power down mode from this state.

STOP

The volume muting function has been cancelled and the timbre data settings have been completed. In this state, FIFO is empty. This state is restored when the melody reproduction is stopped.

Also, the procedure to reduce the power of the digital section can be taken from this state. This state will be restored when the power-down function is cancelled.

PLAY Standby

Writing the musical score data into FIFO has been completed and ready for melody reproduction. Setting "1" for the ST bit will set for the next PLAY mode. It is possible to take the procedure to reduce the power of the digital section from this state. However, the STOP state will be restored after the power-down function is cancelled.

PLAY

The melody is being reproduced. Setting “0” for the ST bit will set to the STOP mode. It is prohibited to change the digital section from this mode to the power down mode. (It may cause noises to occur.)

Digital Power Down mode

The power of the digital section has been reduced. ("1" set for DP bit)

As clocks are not inputted inside of the LSI even when they are inputted to the CLK_I terminal, power consumption of the digital section can be reduced. Before proceeding to this mode, set both HP volume and FM volume to "MUTE".

Operation in FIFO empty state

If FIFO has become empty during reproduction, the musical score data written last is processed continuously until the next data is entered.

If the last written data is a note data, that note is reproduced continuously.

If the last written data is a rest data, the rest state will be maintained.

Reproduction method assuming occurrence of empty state

In the ordinary melody reproduction, it is prohibited to allow the FIFO empty state to occur. However, utilizing the above feature enables short sounds produced easily. The interrupt function would not be necessary.

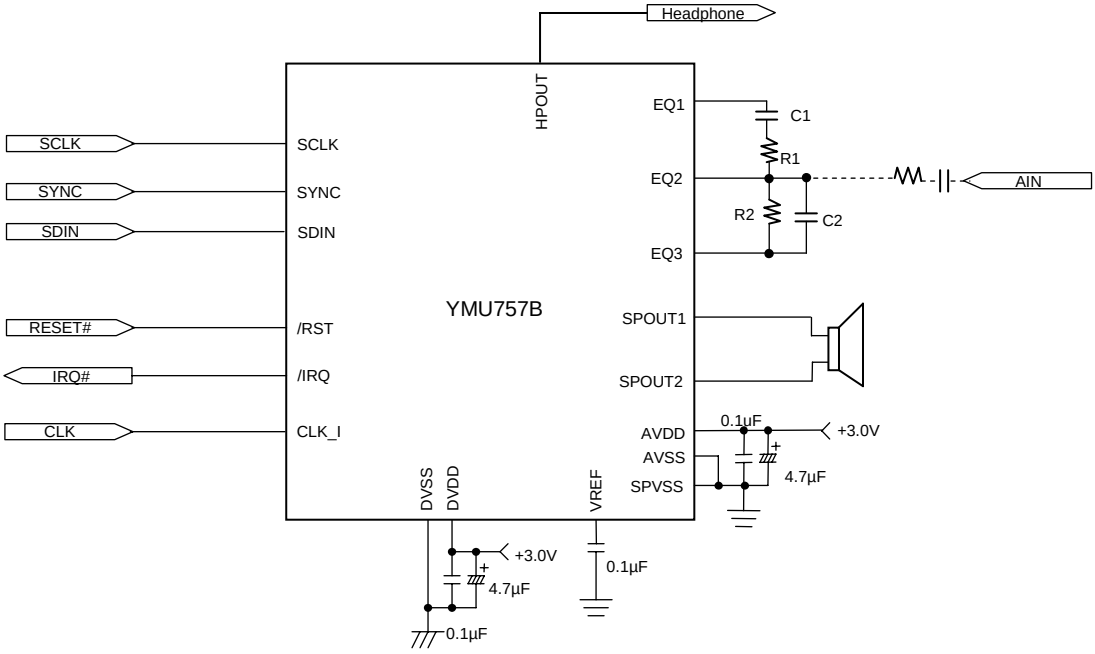
To have short sounds produced, follow the steps as described below.

Short sounds are applicable to 1 to 32 word data block.

If the data block exceeds 33 words, use the regular reproduction procedure utilizing the interrupt function.

1) Complete the procedure of Power ON --> Analog Power Down mode -- Initialized --> STOP in advance. (Please refer to "State transition description " diagram on page 26.)
2) Start reproduction in the FIFO empty state.
3) Write the data block to be reproduced into FIFO.
4) Immediately after writing (after 0 to 20us), the musical score data are processed internally and reproduction is started.
   As reproduction goes on, the data in FIFO are processed and cleared.
5) When FIFO becomes empty, if the last data in the data block is a note data, that note is reproduced continuously and if it is a rest data, the rest state is retained until the next data block is written into FIFO.
6) When reproducing the next data block, go to step 3).
   To stop reproduction, set "0" for ST. Then the data counter of FIFO will be cleared and the state as described in step 1) will be restored.

■ Example of system connection



Warning for the device which makes sound through speaker

A speaker radiates heat in a voice-coil by air flow accompanying vibration of an oscillating board. When DC signal (several Hz or less) is inputted, heat radiation characteristics falls rapidly.

In addition, even if it is used lower than rated input, it may lead to disconnection of a voice-coil, emitting smoke or ignition of a speaker.

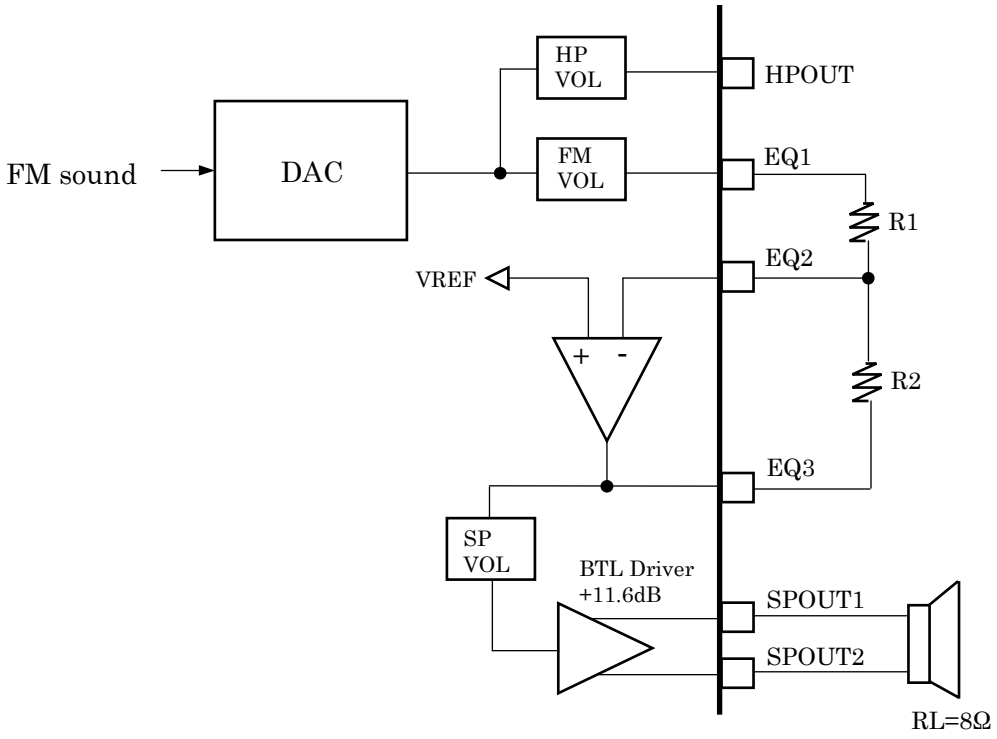
In order to avoid such situations, be sure to implement one or more preventive measures from the following.

1. Do not select a setup (sound production) which may generate DC signal.
   (Since thoroughness of this preventive measure is generally difficult, we recommend the combined use with the following 2, 3, and 4)
2. Add a DC cut digital filter for cutting DC signal into a digital section.
   (As long as "Built-in" is not mentioned in the manual, there is no such built-in circuit inside of a device).
3. Add a DC cut capacitor for cutting DC signal into an analog section.
   (When addition is specified in the example of a recommended circuit diagram, be sure to add)
4. When a latter stage device exists in the signal path from this device to speaker, DC cut is realized in a latter stage device.

In addition, the above-mentioned measures are made that the device it-self, DC cut condenser, and a latter stage device will be in a normal operation. Therefore, it is also necessary to implement the safety measures supposing failure of these parts separately.

■ One sound and volume level adjustment in 4 sound pronunciation

The volume level outputted from DAC by the number of the pronunciation is different.
When 1 sound (*) is outputted from FM sound source, output voltage amplitude from DAC is 0.375Vp-p.
When more than one sound is pronounced at the same time, output voltage amplitude varies in the phase of each wave shape.
But, when the wave shape of the same phase piles up, it becomes 0.75Vp-p by 2 sound, 1.125Vp-p by 3 sound, 1.5Vp-p by 4 sound.
(*: The volume adjustment (Total Level of Carrier) of 1 sound is being explained with the premise of 0dB.)



An assumption in 300m W output.

Output power from the speaker is 300mW when RL is 8Ω and a voltage between SPOUT1 and 2 is 1.55Vrms.
BTL output amplitude at this time becomes 1.55×2×1.414=4.38Vpp, and becomes 4.38/3.8=1.15Vpp with the EQ3 terminal.
(Gain with the speaker amplifier is +11.6dB= 3.8 times.)

Securing a volume level by one sound.

Gain adjustment in the part EQ amplifier is recommended as the way of securing a volume level by one sound.
Gain depends on the resistance ratio of R1 and R2, and it is GAIN=R2/R1.
Gain to recommend is about four times from three times.

A level adjustment recommendation example in all

FM volume or either of SP Volumes is a little squeezed as a default (from –3dB to -6dB).
When a user adjusts volume, it is considered controlling either FM or SP volume.
At this time, because the side which gain is raised to is secured in advance, either of FM volume or SP Volumes is a little squeezed as a default.
It is recommended making gain of the part EQ amplifier about 3 - 4 times to secure the output level for which to be one sound (For example, R1=22kΩ, R2=82kΩ).
When one sound is pronounced under this condition(FM volume as 0dB), EQ1 is 0.375Vp-p.
In this state, if set gain=four times in EQ amplifier, EQ3 becomes 1.5Vp-p.
When it is set up in -4dB with SPVOL, voltage between SPOUT1 and 2 becomes 3.6Vp-p, and can be get output power 162mW with the speaker (RL=8Ω).

A level adjustment of four sound pronunciation simultaneously

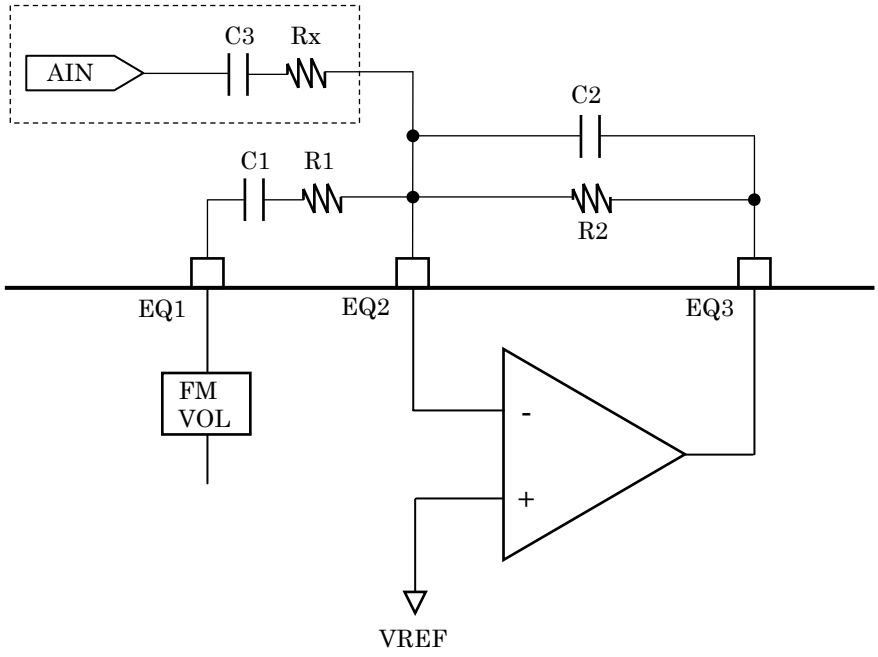
When usual music is regenerated, the amplitude of DAC never almost swings to 1.5Vp-p.
Therefore, there is no hindrance by the setup of GAIN which is the same as 1 sound.
Adjust it with FM, SP Volume if you restrain GAIN of the part EQ amplifier a little when you are anxious about the distortion of the sound.

A level adjustment of HPOUT

Adjust it outside the LSI when you raise gain on the HPOUT side.

■ Sound quality correction circuit

It is possible to correct the sound quality and gain by using an external circuit connected to EQ1 to 3 terminals.
A circuit structure of EQ1 to 3 terminal inside and example of external circuit are as follows.

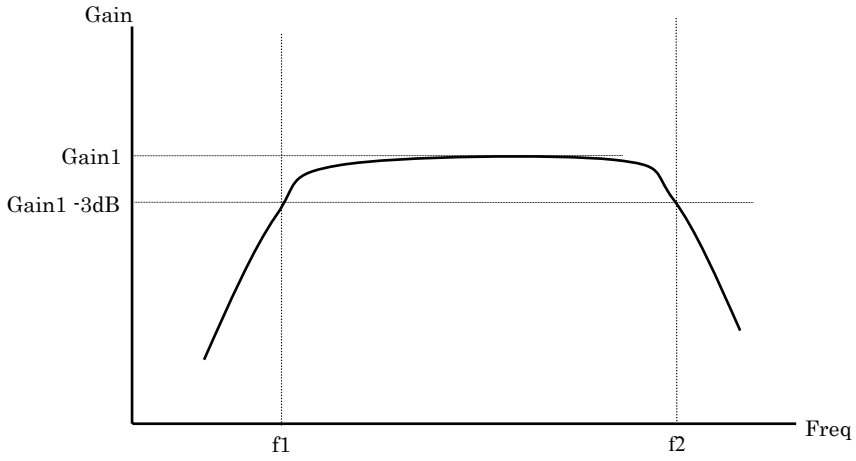


Gain and filter characteristic are adjusted by value of C1, C2, R1 and R2.
Gain = R2 / R1. Recommendation of R1 is 22kΩ and R2 is 82kΩ (gain = 3.7 times).
Cut off frequency f1 and f2 of filter is as follows.

$f1=1/(2\pi \times R1 \times C1)$.

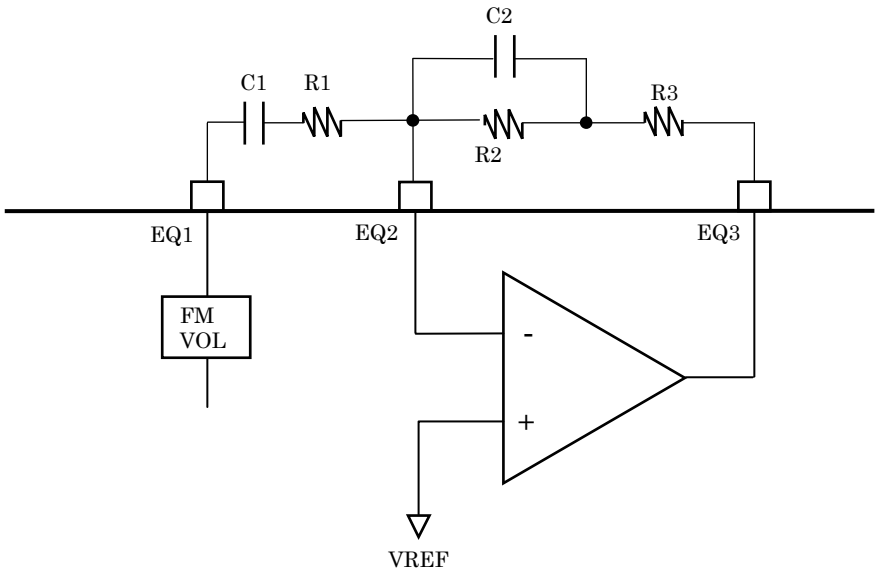
$f2=1/(2\pi \times R2 \times C2)$.

Recommendation of each value are as follows.
If C1=0.022µF and C2=120pF, cut off frequency f1=330Hz and f2=16kHz.



Moreover, the circuit enclosed with the dotted line becomes necessary when an analog signal is inputted from AIN and it wants to mix it.
The level adjustment that it is mixed depends on the resistance ratio R2/Rx of Rx and R2.
The value of Rx when it wants to mix it in the amplitude of one time of AIN is 82kΩ.

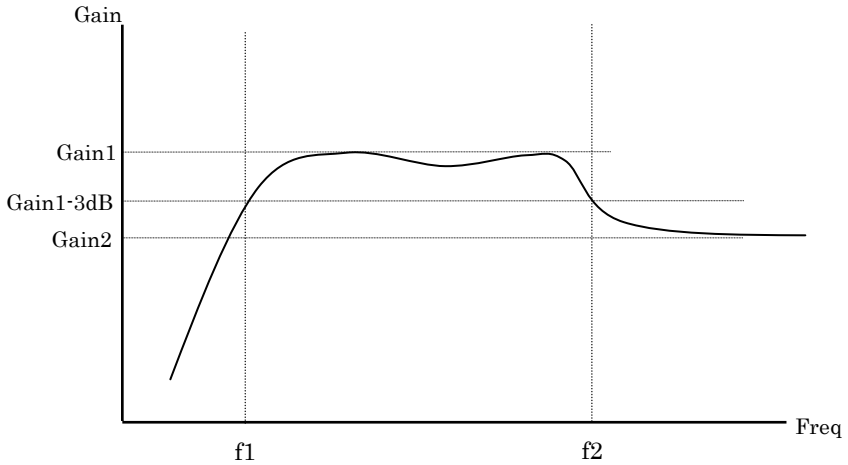
If add resister R3, frequency characteristic is as follows.



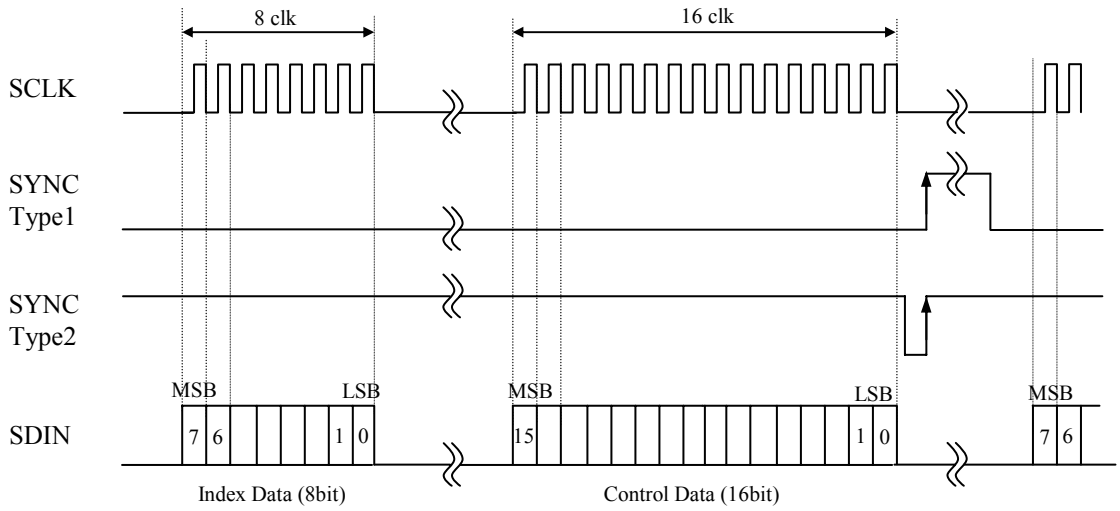
Gain1= (R2+R3) /R1. Gain2=R3/R1.
Cut off frequency f1 and f2 of filter is as follows.

f1=1/ (2π×R1×C1).

f2=1/ (2π×R2×C2).



Serial I/F Specifications



The YMU757B is controlled through the three serial interfaces SCLK, SYNC and SDIN.

About the relations between SDIN and SCLK

The value of SDIN is taken in the inside of the LSI at the SCLK rise.
Input SDIN so that setup/Hold time is secured to rise edge of SCLK.
(Refer to the AC characteristics of the electric characteristics for the details of the timing specification.)

About SDIN

The figure above shows no data transmission between Index data and Control data but it means nothing problematic. 24 bit continuous data transmission is also possible.
When transmitting the data by 8-bit unit, transmit the upper 8 bits and lower 8 bits of the control data separately. There is no particular specification for the interval between the end of transmission of the upper 8 bits and start of transmission of the lower 8 bits. However, the longer the interval is, the longer time one transmission takes. When entering the musical score data into FIFO, use care not to make FIFO empty.

About SYNC

It can correspond to Type1 and Type2 of the upper figure.
When rise edge of SYNC occurs inside the LSI, it considers that the data transfer of one time was completed.
SDIN for 24×SCLK just before rise edge of SYNC occurs is judged valid data.
(SDIN for 16×SCLK are valid data when transfer only Control Data.)
There is no regulation specially about the length of the H period.
But, L period is to make 100ns be secured at least in the case of the Type2 wave shape
It has the possibility that faulty operation is caused when rise edge of SYNC and fall edge of SCLK approach it.
Give careful consideration to rise edge of SCLK doesn't occur toward rise edge of SYNC.

About the data transfer only Control Data.

If input SDIN for SCLK×16 between rise edge of SYNC and next rise edge of SYNC, the inside of the LSI is judged it is music data ($00h) and take it.

Electrical characteristics

1. Absolute maximum ratings

Parameter	Symbol	Min.	Max.	Unit
Power supply voltage (analog)	AV_{DD}	-0.3	4.2	V
Power supply voltage (digital)	DV_{DD}	-0.3	4.2	V
Analog input voltage	V_{INA}	-0.3	AV_{DD}+0.3	V
Digital input voltage	V_{IND}	-0.3	DV_{DD}+0.3	V
Operating temperature	T_{OP}	-20	85	°C
Storage temperature	T_{STG}	-50	125	°C

Note) DV_{SS} = AV_{SS}= SPV_{SS} = 0V

2. Recommended operating conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating voltage (analog)	AV_{DD}	2.7	3.0	3.3	V
Operating voltage (digital)	DV_{DD}	2.7	3.0	3.3	V
Operating temperature	T_{OP}	-20	25	85	°C

Note) DV_{SS} = AV_{SS} = SPV_{SS} = 0V

3. DC characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High-level input voltage	V_{IH}		0.7 × DV_{DD}	-	-	V
Low-level input voltage	V_{IL}		-	-	0.2 × DV_{DD}	V
High-level output voltage	V_{OH}	I_{OUT} = -1mA	0.8 × DV_{DD}	-	-	V
Low-level output voltage	V_{OL}	I_{OUT} = 1mA	-	-	0.4	V
Schmitt width	Vsh			1.0		V
Input leakage current	IL		-10		10	μA
Input capacity	CI				10	pF

Note) T_{OP}=-20~85°C, DV_{DD}=3.0±0.3V, Capacitor load=50pF

4. AC characteristics

Input V_{IH}=0.8×DV_{DD}, V_{IL}=0.1×DV_{DD} as input signal. Measure timing at V_{IH}=0.7×DV_{DD}, V_{IH}=0.2×DV_{DD}.

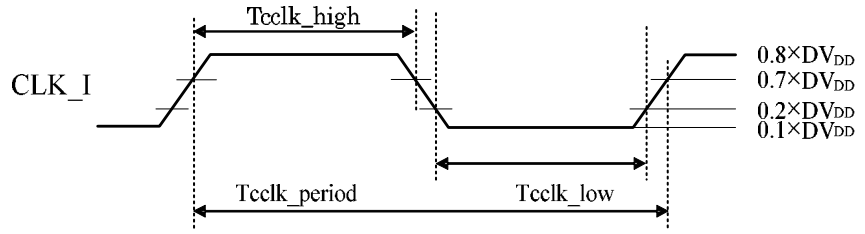
4-1. CLK_I ,Reset

Parameter	Symbol	Min.	Typ.	Max.	Unit
CLK_I clock cycle period	Tcclk_period	35.8			ns
CLK_I "L" pulse width	Tcclk_low	12			ns
CLK_I "H" pulse width	Tcclk_high	12			ns
/RST active "L" pulse width	Trst_low	100			× CLK_I
SCLK start delay time (after /RST inactive)	Trst2clk	64			× CLK_I

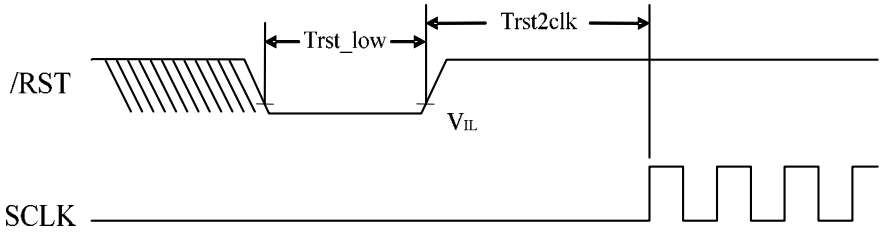
Note) T_{OP}=-20~85°C, DV_{DD}=3.0±0.3V, Capacitor load=50pF

× CLK_I means the number of clocks inputted through the CLK_I terminal.

CLK_I Duty



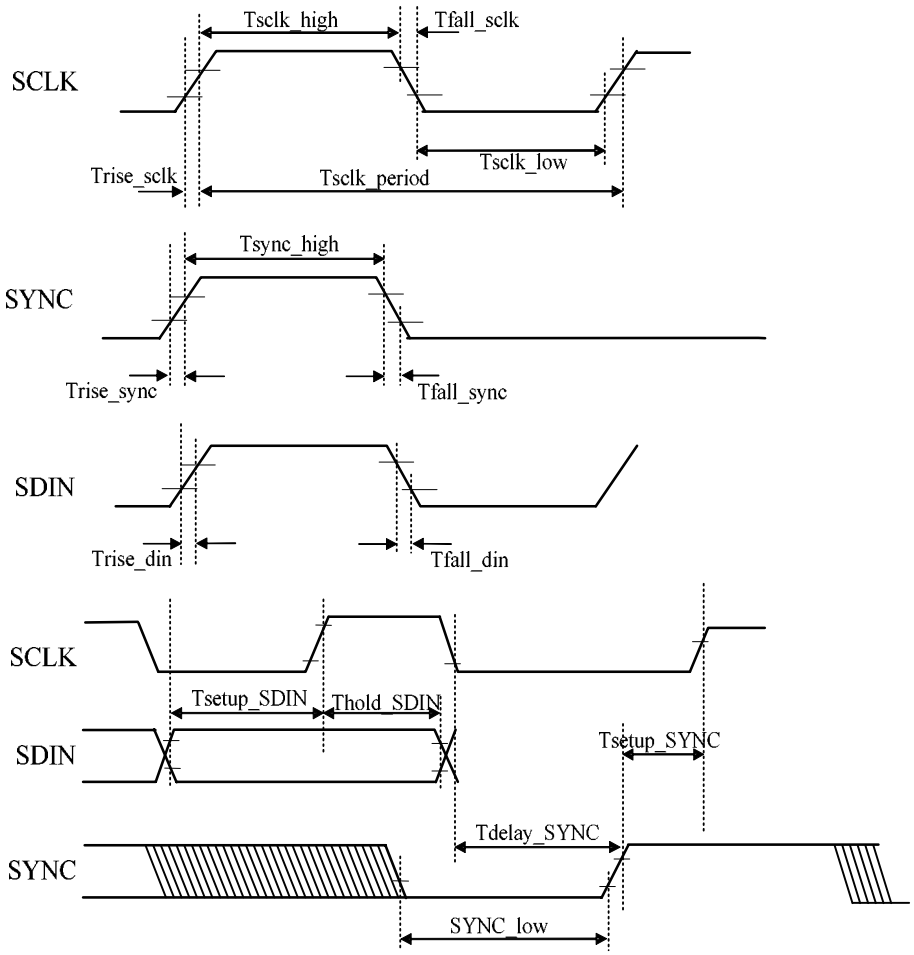
Hardware Reset



4-2. Serial Interface

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCLK clock period	Tsclk_period	430		-	ns
SCLK "L" pulse width	Tsclk_low	200			ns
SCLK "H" pulse width	Tsclk_high	200			ns
SCLK rise time	Trise_sclk	-	-	20	ns
SCLK fall time	Tfall_sclk	-	-	20	ns
SYNC "H" pulse width	Tsync_high	100		-	ns
SYNC rise time	Trise_sync	-	-	20	ns
SYNC fall time	Tfall_sync	-	-	20	ns
SYNC delay time	Tdelay_SYNC	0			ns
SYNC “L” pulse width	SYNC_low	100	-	-	ns
SYNC > SDIN setup time	Tsetup_SYNC	50	-	-	ns
SDIN setup time	Tsetup_SDIN	50	-	-	ns
SDIN hold time	Thold_SDIN	50	-	-	ns
SDIN rise time	Trise_din	-	-	20	ns
SDIN fall time	Tfall_din	-	-	20	ns

Note) T_{OP}=-20~85°C, DV_{DD}=3.0±0.3V, Capacitor load=50pF



5. Power consumption

Parameter	Min.	Typ.	Max.	Unit
During normal operation (digital)		500	2000	μA
During no output sound(analog)		9	12	mA
Output 300mW (analog) (RL=8Ω)		200	300	mA
In power-down mode		0.1	1	μA

Note) T_{OP}=-20~85°C, DV_{DD}= AV_{DD} = 3.0±0.3V, Capacitor load=50pF

6. Analog characteristics

SP Amplifier

Parameter	Min.	Typ.	Max.	Unit
Gain setting (fixed)		±1.9		times
Minimum resister load (RL)		8		Ω
Full-scale analog output(RL=8Ω)		5.0		Vp-p
Maximum output power (RL=8Ω,THD+N<=0.05%)		360		mW
Maximum output power (RL=8Ω,THD+N<=1.0%)		400		mW
THD + N (RL=8Ω,f=1kHz,300mW output)		0.025		%
Noise level(no signal, f= 400Hz - 20kHz)		-90		dBV
PSRR (f=1kHz)		65		dB

Note) T_{OP}=25°C, DV_{DD} = AV_{DD} = 3.0V

EQ Amplifier

Parameter	Min	Typ	Max.	Unit
Gain setting range			30	dB
Maximum output current	120			μA
Full-scale analog output		1.5		Vp-p
THD + N (f=1kHz)			0.01	%
Noise level (no signal, f= 400Hz - 20kHz)		-90		dBV
Input impedance	10			MΩ
PSRR (f=1kHz)		36		dB

Note) T_{OP}=25°C, DV_{DD} = AV_{DD} = 3.0V

SP Volume

Parameter	Min	Typ	Max	Unit
Volume setting range	-30		0	dB
Volume step width		1		dB
Noise level (no signal, f= 400Hz - 20kHz)		-90		dBV
THD + N (f=1kHz)			0.01	%

Note) T_{OP}=25°C, DV_{DD} = AV_{DD} = 3.0V

FM Volume

Parameter	Min	Typ	Max	Unit
Volume setting range	-30		0	dB
Volume step width		1		dB
Noise level (no signal, f= 400Hz - 20kHz)		-90		dBV
Maximum output current	120			μA
Full-scale analog output		1.5		Vp-p
Output impedance		300	600	Ω
PSRR (f=1kHz)		36		dB

Note) T_{OP}=25°C, DV_{DD} = AV_{DD} = 3.0V

HP Volume

Parameter	Min	Typ	Max	Unit
Volume setting range	-30		0	dB
Volume step width		1		dB
Noise level (no signal, f= 400Hz - 20kHz)		-90		dBV
Maximum output current	120			μA
Full-scale analog output		1.5		Vp-p
Output impedance		300	600	Ω
PSRR (f=1kHz)		36		dB

Note) T_{OP}=25°C, DV_{DD} = AV_{DD} = 3.0V

VREF

Parameter	Min	Typ	Max	Unit
VREF voltage	1.4	1.5	1.6	V

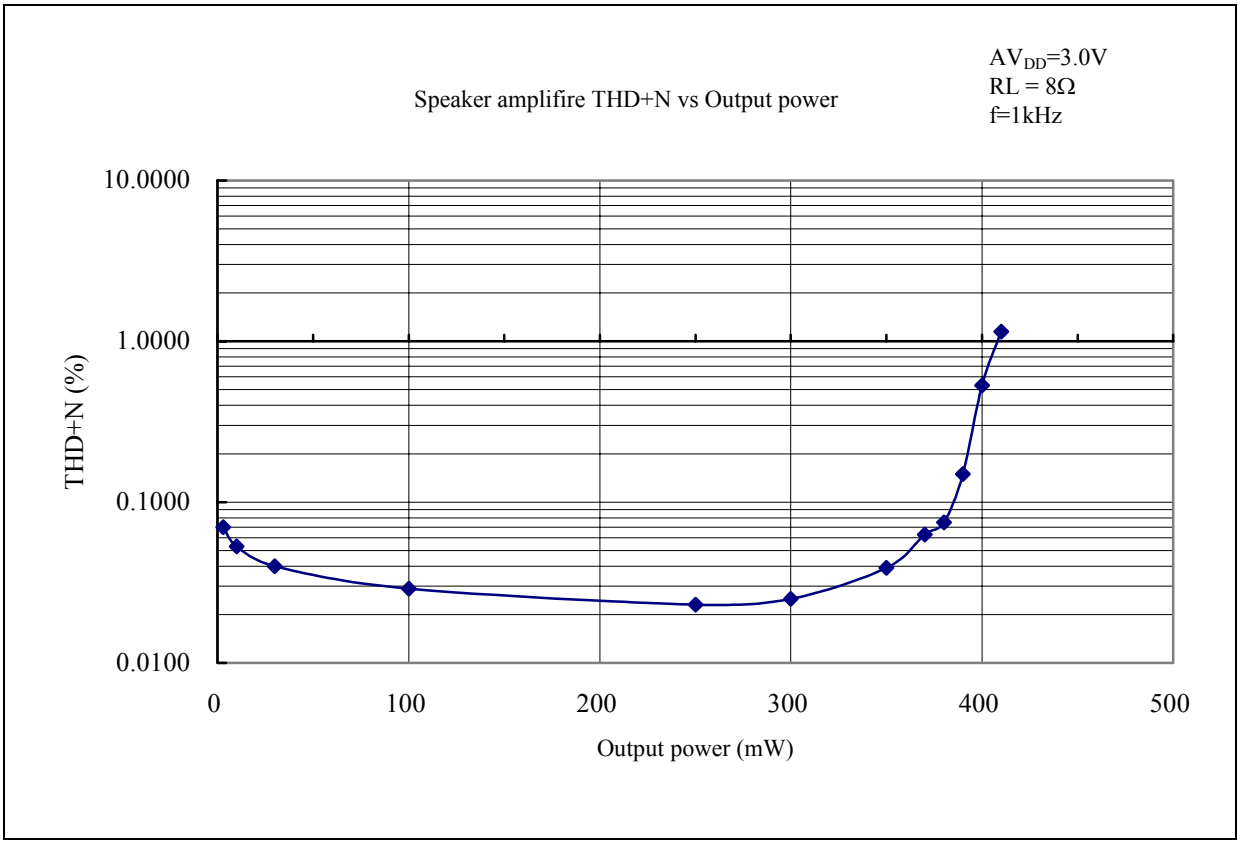
Note) T_{OP}=25°C, DV_{DD} = AV_{DD} = 3.0V

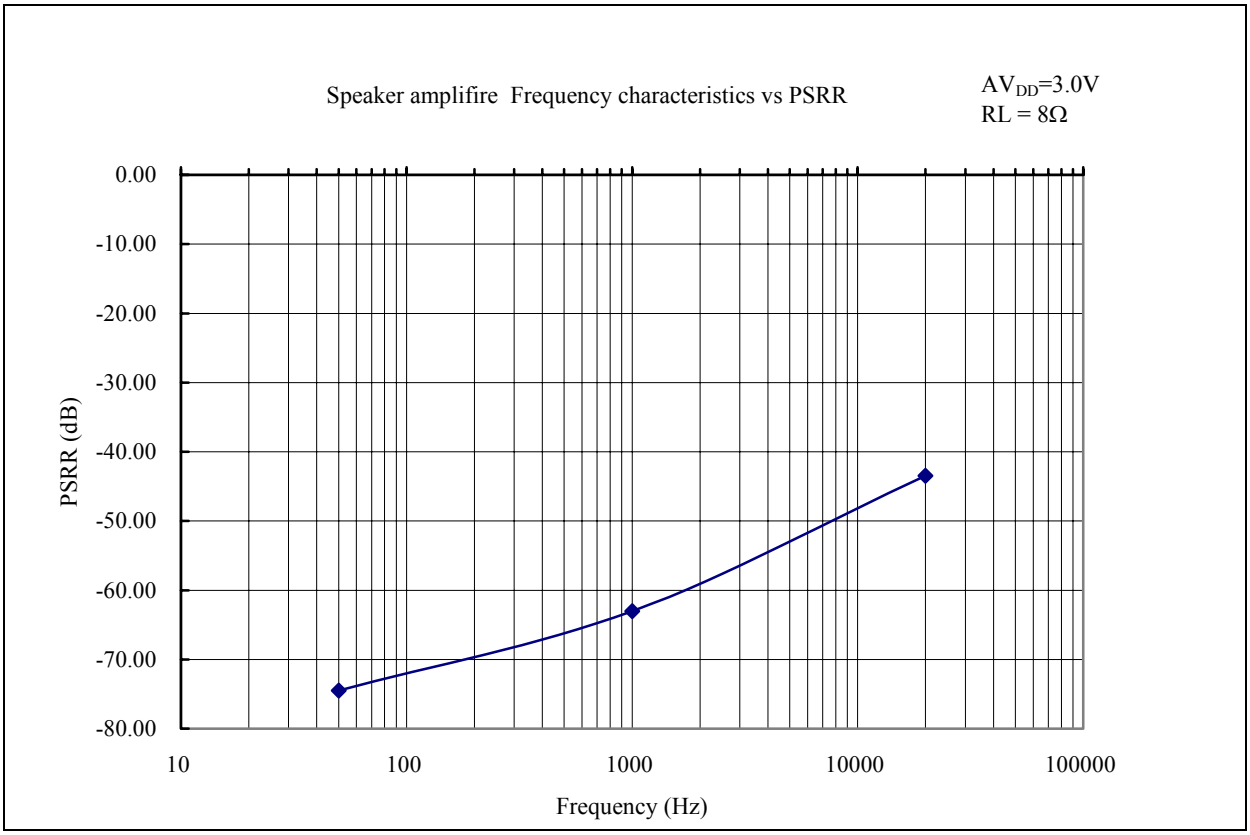
DAC

Parameter	Min	Typ	Max	Unit
Resolution		12		Bit
Full-scale analog output (*)		1.5		Vp-p
THD+N (f= 1kHz)			0.5	%
Noise level (no signal, f=400Hz - 20kHz)		-90		dBV
Frequency characteristic (f=50Hz - 20kHz)	-0.5		+0.5	dB

Note) T_{OP}=25°C, DV_{DD} = AV_{DD} = 3.0V

* When it was made to pronounce FM 4 sound at the same time in the same phase.


Speaker amplifire THD+N vs Output power
AVDD=3.0V
RL = 8Ω
f=1kHz
10.0000
1.0000
0.1000
0.0100
THD+N (%)
0
100
200
300
400
500
Output power (mW)


Speaker amplifire Frequency characteristics vs PSRR
AVDD=3.0V
RL = 8Ω
0.00
-10.00
-20.00
-30.00
-40.00
-50.00
-60.00
-70.00
-80.00
PSRR (dB)
10
100
1000
10000
100000
Frequency (Hz)

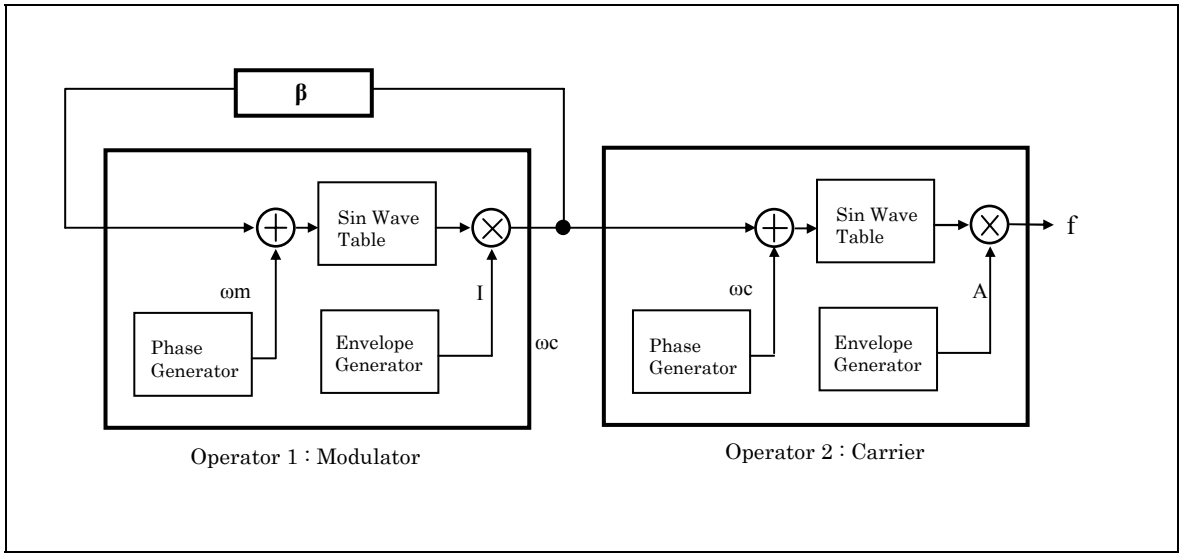
■ General description of FM sound generator

"FM" stands for Frequency Modulation.

The FM sound generator utilizes the higher harmonic wave produced by the frequency modulation for synthesis of the musical sounds

As use of this FM system enables a comparatively simple circuit to produce such waveform that has a harmonic wave including disharmonious sounds, it is possible to create a wide range of sounds from the synthesized sounds of the natural musical instruments to the electronic sounds.

The diagram below shows the most basic configuration of the FM system.



The "Operator" refers to the section where a sine wave is generated and the combination of the operators is called "algorithm". The operator in the front stage is called "modulator" and that in the rear stage "carrier".

Each operator is capable of setting the frequency and the envelope waveform.

The configuration in the above diagram can be expressed in the formula as follows.

$$FM(t) = A \sin(\omega c t + B \sin \omega m t)$$

A : Amplitude of the carrier. B : Amplitude of the modulator. ωc : Angle frequency of the carrier

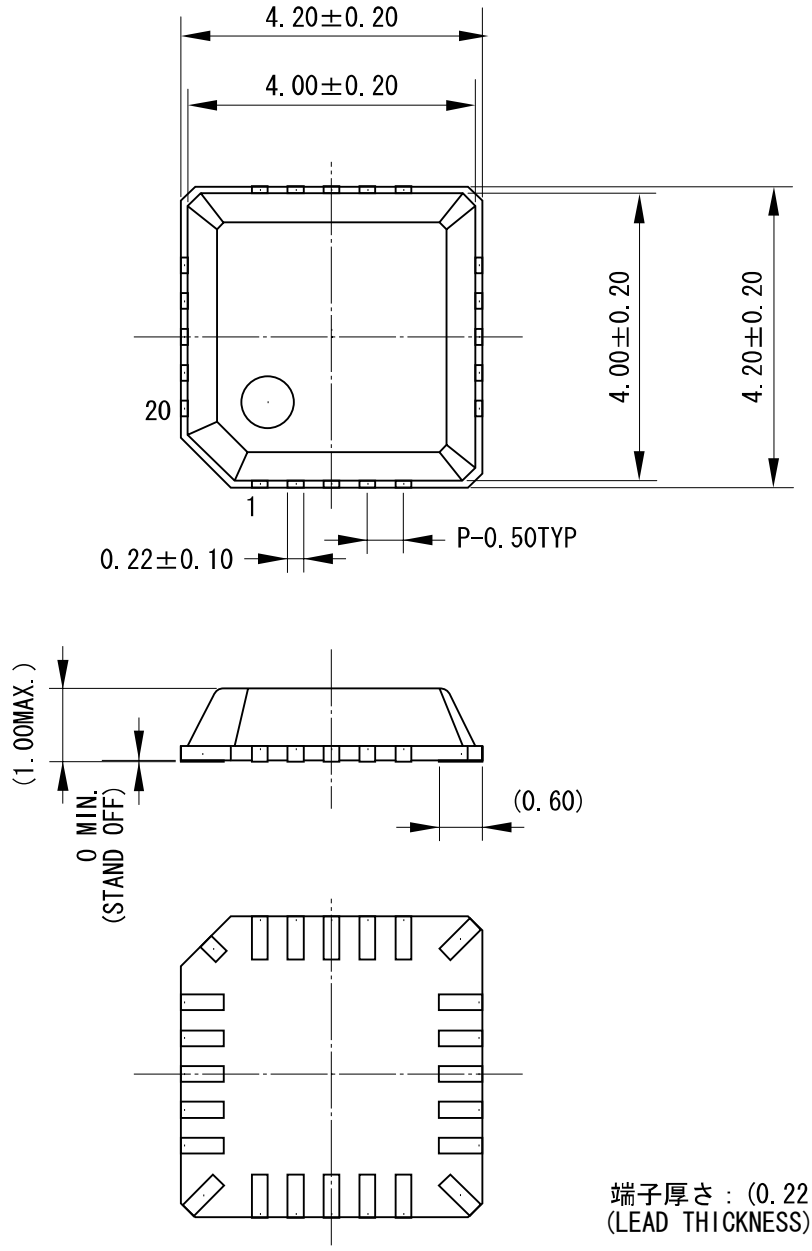
ωm : Angle frequency of the modulator

In addition, a system called "feedback FM" is available to create a wider range of sounds. In this system, the frequency modulation is fed back as shown in the diagram in the following page.

B is called "feed-back ratio". Using the feed-back FM function, it is possible to produce the strings type sounds.

■ External dimensions

C-PK20QP-2



モールドコーナー形状は、この図面と若干異なるタイプもあります。
カッコ内の寸法値は参考値です。
モールド外形寸法はバリを含みません。
単位： mm

The shape of the molded corner may slightly differ from the shape in this diagram.
The figure in the parentheses ( ) should be used as a reference.
Plastic body dimensions do not include resin burr.
UNIT: mm

注） 表面実装LSIは、保管条件、及び半田付けについての特別な配慮が必要です。
詳しくはヤマハ代理店までお問い合わせください。

Note: The storage and soldering of LSIs for surface mounting need special consideration.
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