# Input / Output Buses

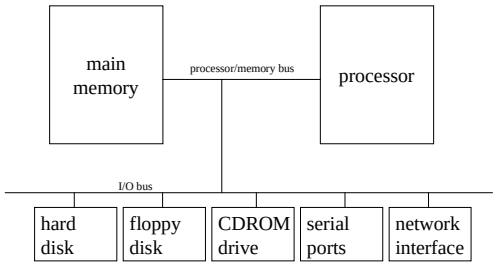
CSE 410 - Computer Systems
October 31, 2001

## Readings and References

- Reading
  - Sections 8.4, 8.5, *Computer Organization & Design*, Patterson and Hennessy
- Other References



## A typical organization






## Constraints

- Two primary design points that must be met
- High speed
  - processor to memory
- Flexibility
  - many types of I/O devices with widely varying characteristics
  - characteristics of future devices are unknown at design time



## Designs

- The speed and flexibility constraints lead to designs which are
  - designed for speed
    - processor-memory bus
  - designed for flexibility
    - I/O bus
  - designed for both
    - backplane bus



## Speed - Synchronous Bus

- For highest speed, all devices are designed to work together at the same high rate
- Synchronous buses have a clock signal that all devices on the bus are aware of
- Protocol for accessing the bus is relatively simple
  - control signals at specified clock cycles
  - data at specified clock cycles

## Synchronous Issues

- Runs fast
- but
  - all attached devices must be designed for this particular (probably proprietary) bus
  - must be short so that signals can propagate across the whole bus
  - fast today is slow tomorrow



## Flexibility - Asynchronous Bus

- Devices access the bus by handshaking to determine who can go next
- No single clock
  - transactions are defined by control signal transitions
- Can accommodate a wide variety of device speeds and device types



## Asynchronous Issues

- Flexible
- but
  - the handshake adds overhead to each transfer
  - special cases pollute the protocol as it is extended to provide higher speed capabilities
  - extreme network effect: once a bus is popular, it lives long past its expected lifetime because there are so many devices that use it



## Bus Bandwidth

- Width of the bus
  - number of data lines can be increased to transfer more bits of data in parallel
- Multiplexing
  - data lines and control lines can be separated to allow overlapped handshake and data transfer
- Multi-word transfers
  - block transfers move more data per handshake



## Controlling bus access

- With multiple devices on the bus, something must control access
- Bus Master
  - device that is allowed to initiate transfers
- Single bus master
  - simple, because no contention
  - potential bottleneck, because one device is busy for every single transfer on the bus



## Multiple Masters and Arbitration

- Let several devices act as bus masters
- Must decide who is in control for any particular transaction
- Arbitration
  - daisy chain - serial decision
  - centralized parallel - one decider
  - distributed parallel - many deciders
  - distributed with collision detection