CSE390C Autumn 2014 – Quiz 2 (19 November)

Name:

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1. Verilog to state machine (10 points)

A. Given the following VERilog code, draw a schematic with FFs and gates/wires connecting them.

```verilog
module problem_1 (clk, A, B, C)
    output A, B, C;
    input clk;
    reg A, B, C;

    always @(posedge clk) C <= B;
    always @(posedge clk) B <= A;
    always @(posedge clk) A <= A ^ (B ^ C);
endmodule
```

B. If the counter starts with A = 0, B = 0, and C = 1, what are the bit patterns (ordered ABC) we can expect to see at the FF outputs.
2. State machine to Verilog (20 points)

Derive the Verilog for a state machine that takes 2 inputs and generates a single-cycle pulse on its output when the two inputs are the same for two consecutive cycles. You do not need to create a state diagram to solve this problem.