

CSE 390B, Winter 2022

Building Academic Success Through Bottom-Up Computing

Sequential Logic, Bloom's Taxonomy

We hope you had a great MLK weekend!

Bloom's Taxonomy, Cornell Note-Taking Method, Circuit Design, Physical Timekeeping, Sequential Logic

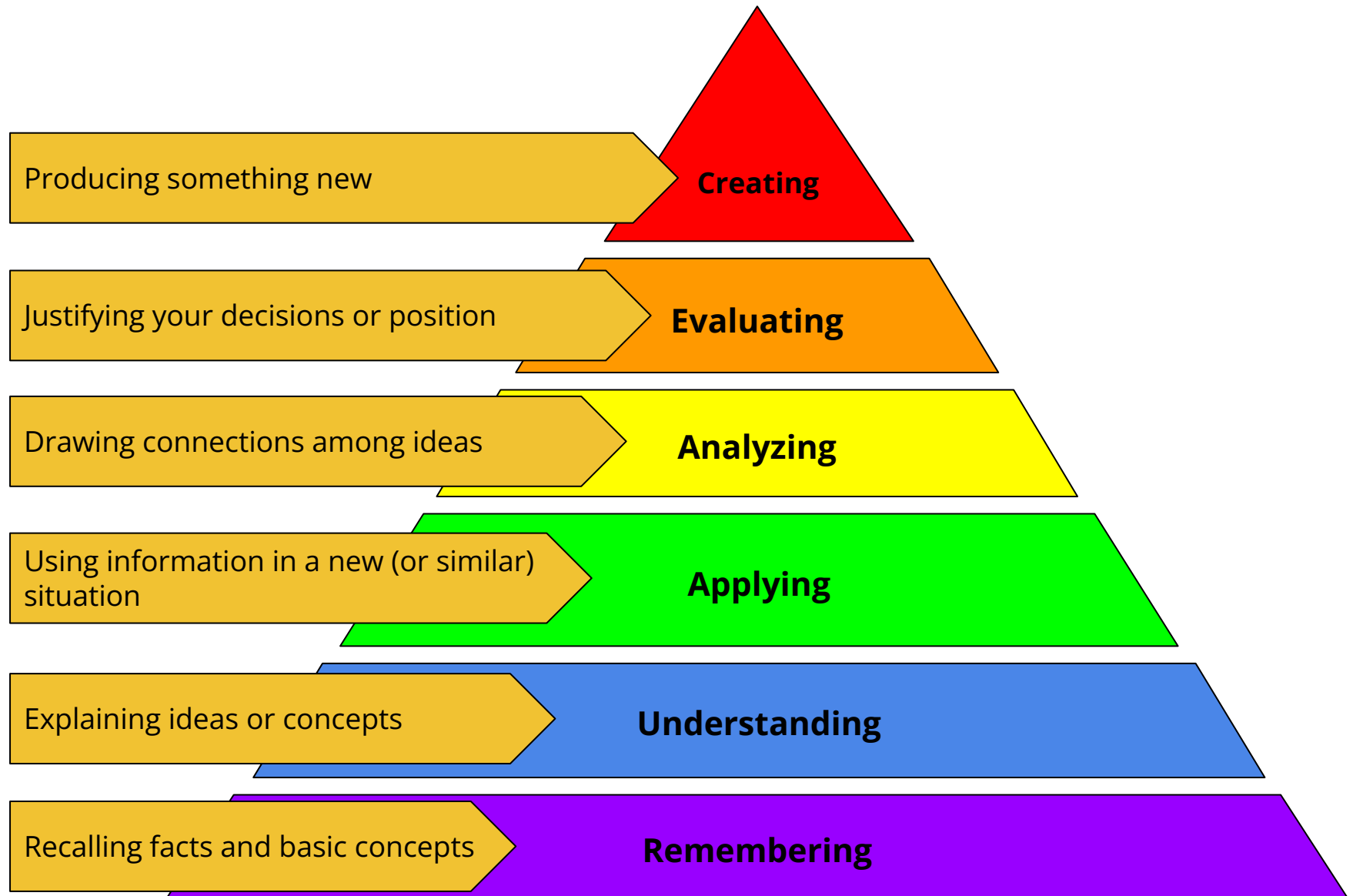
If you are joining virtually, please have your camera turned on!



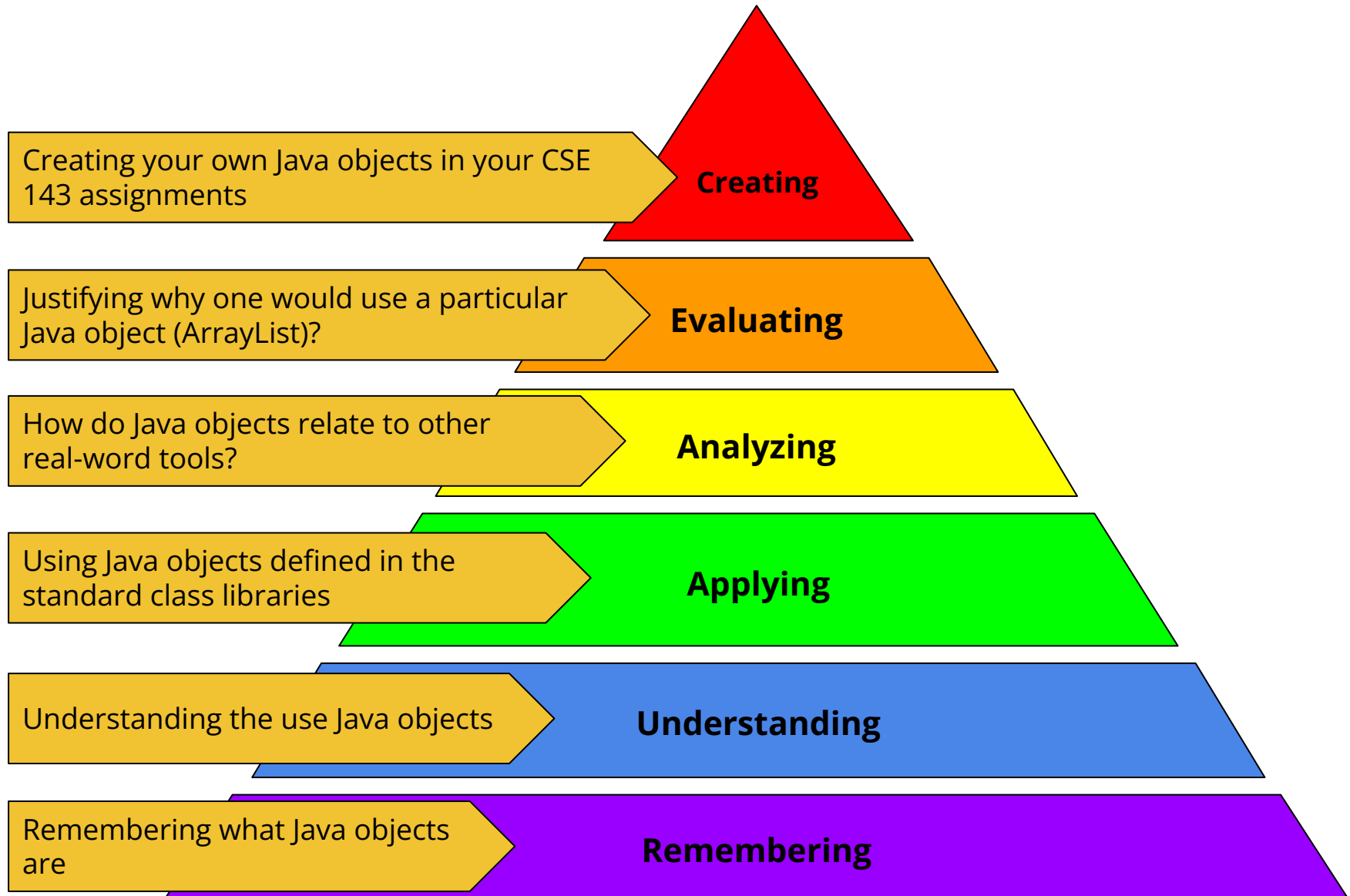
Lecture Outline

- ❖ **Bloom's Taxonomy**
 - Apply levels of learning to coursework
- ❖ Cornell Note-Taking Method
 - System for taking, organizing, and reviewing notes
- ❖ Representing Time in Hardware
 - Sequential Logic vs. Combinational Logic
 - Adding a clock
- ❖ Sequential Logic
 - Data Flip-Flip (DFF) implementation and examples

Bloom's Taxonomy



Bloom's Taxonomy in Action



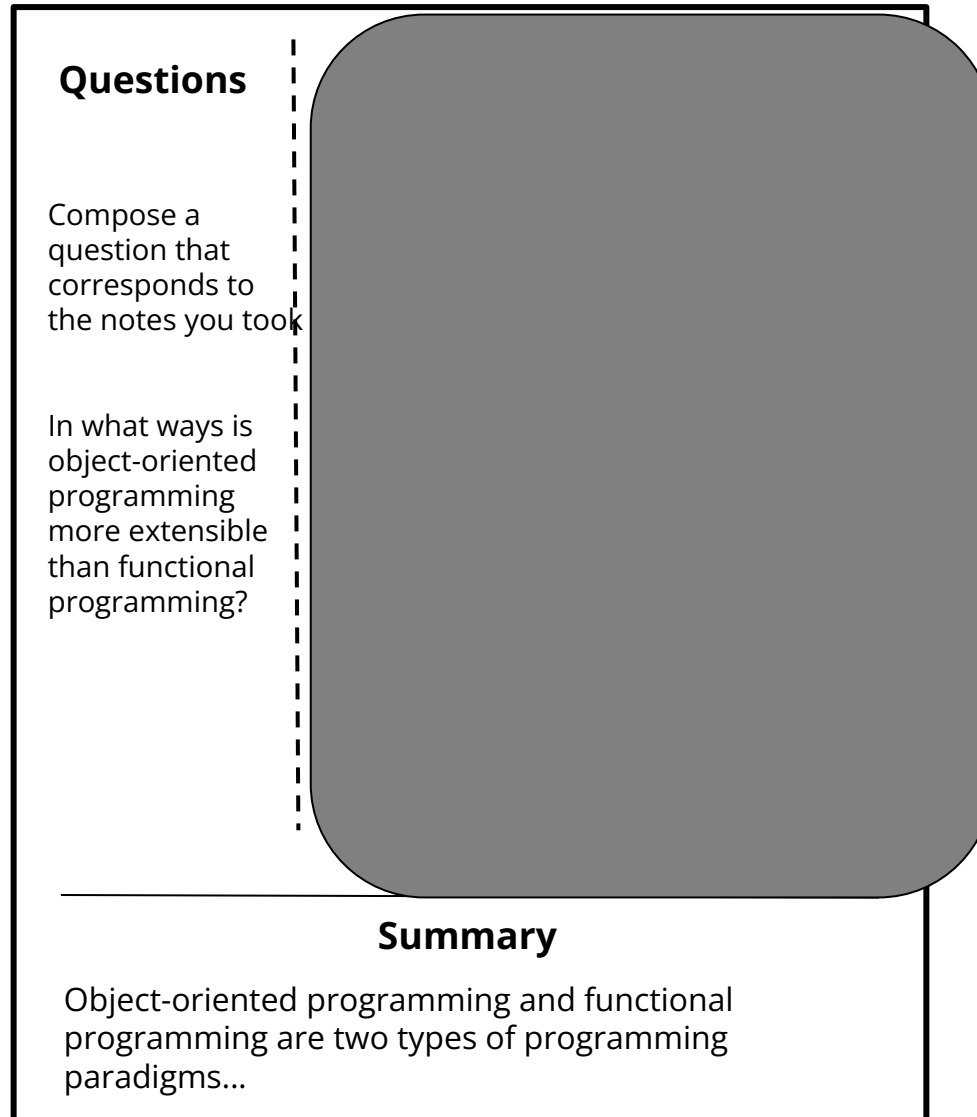
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Cornell Note-Taking Method

Questions	Notes
Compose a question that corresponds to the notes you took	I. Main Topic <ul style="list-style-type: none">○ Sub point○ <u>definition</u>○ example **
In what ways is object-oriented programming more extensible than functional programming?	II. Object-Oriented Programming <ul style="list-style-type: none">○ Encapsulates the data and the operations for a given data type○ Provides abstractions - you don't need to know how a car is implemented in order to use it○ Extensibility - easier to <u>add new data types</u>
	III. Functional Programming <ul style="list-style-type: none">○ Extensibility - easier to <u>add new operations</u>
<hr/> Summary	
Object-oriented programming and functional programming are two types of programming paradigms...	

Cornell Note-Taking Method



Applying the Cornell Note-Taking Method

- ❖ You are going to try it... TODAY!
- ❖ Thursday you will come & contrast Cornell notes with your classmates
- ❖ You are also going to try it with one of your other classes as part of Project 3 (more on Thursday)

Lecture Outline

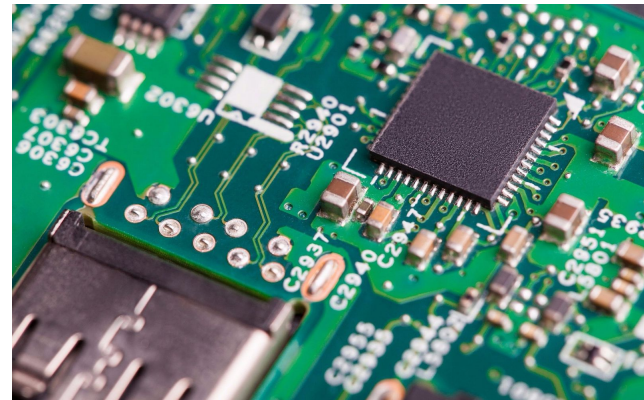
- ❖ Bloom's Taxonomy
 - Apply levels of learning to coursework
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 - **Adding a clock**
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Combinational vs. Sequential Logic

- ❖ So far, we have ignored “time” in our circuits
- ❖ Our chips use **combinational logic**
 - When given inputs, the chip computes its output instantaneously
 - The output is a function of the current inputs, with no memory of previous events
- ❖ Today, we'll start exploring what happens when we consider time, ultimately building to **sequential logic**

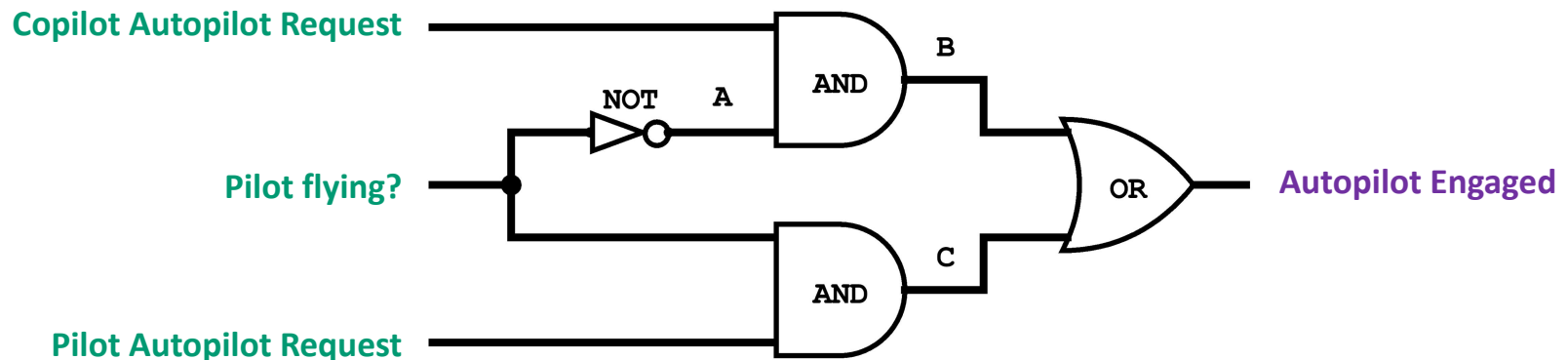
Why Consider Time Now?

- ❖ Needed for our abstraction
 - We need to talk about hardware maintaining state for memory
 - We need vocabulary to talk about time
- ❖ Needed for our implementation
 - Physical implementations of chips cannot be instantaneous
 - We need to account for physical delays in signal propagation



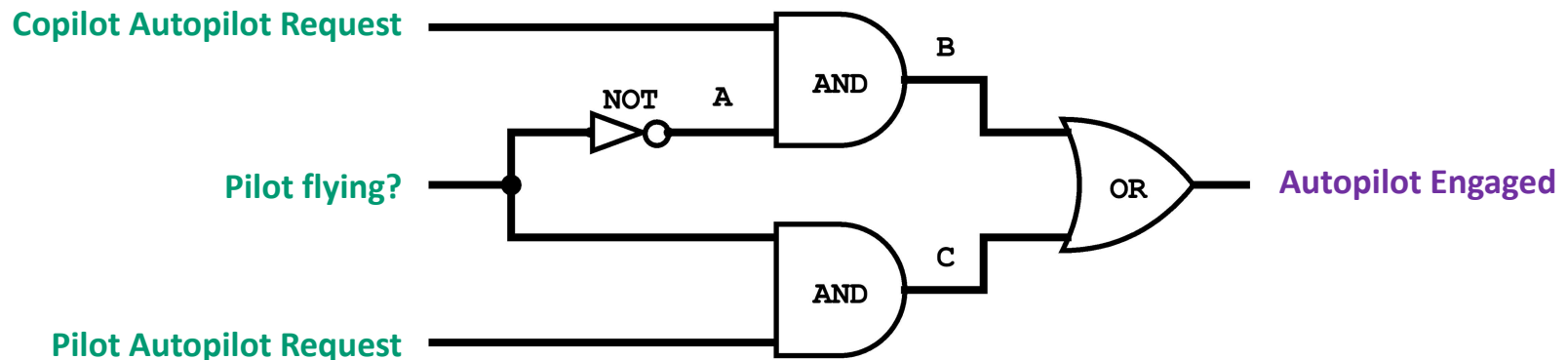
Why Consider Time Now?

- ❖ Consider this autopilot control circuit:
 - Either the pilot or copilot is flying at any time
 - The pilot and copilot can separately request autopilot
 - Only the person flying can request autopilot



Why Consider Time Now?

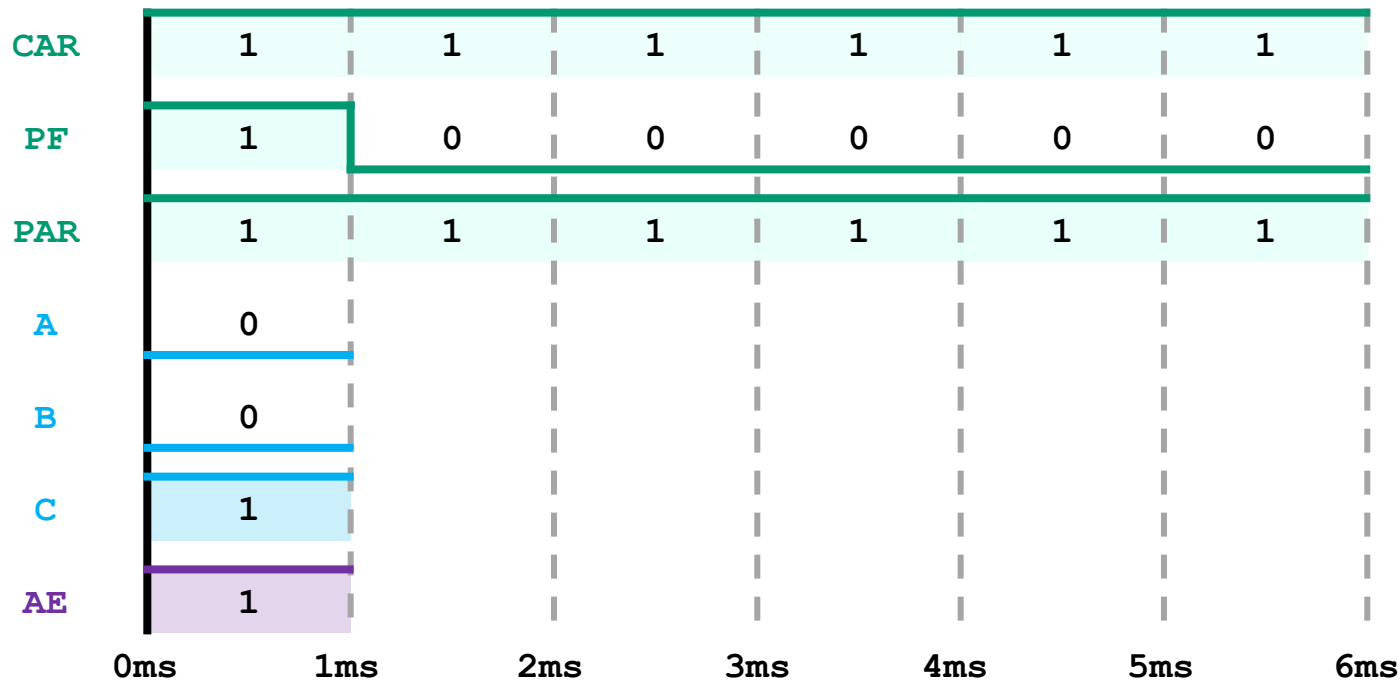
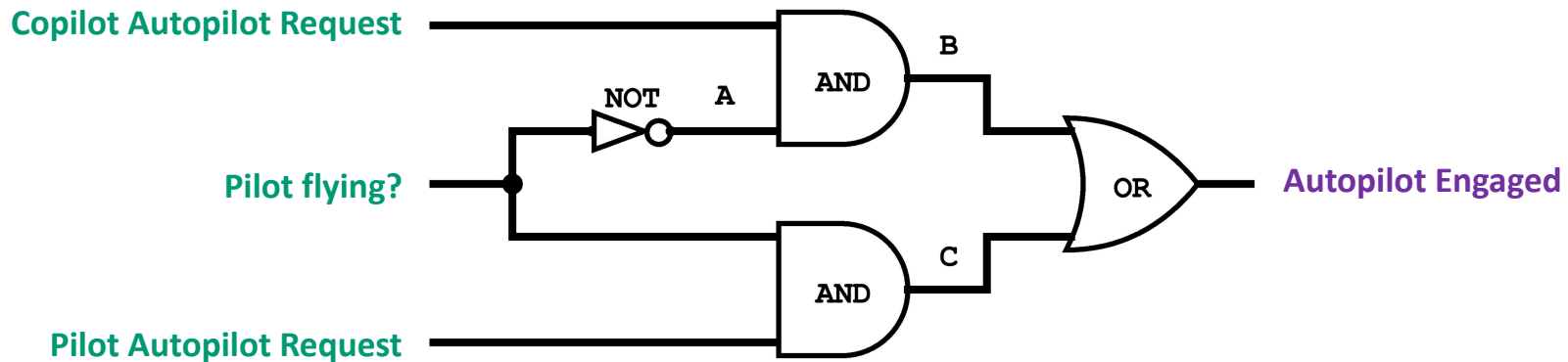
- ❖ Consider this autopilot control circuit:
 - Either the pilot or copilot is flying at any time
 - The pilot and copilot can separately request autopilot
 - Only the person flying can request autopilot



- ❖ Let's assume every logic gate takes 1ms to compute
 - For example, if an input changes at $t=4\text{ms}$, the gate will only output the new result at $t=5\text{ms}$

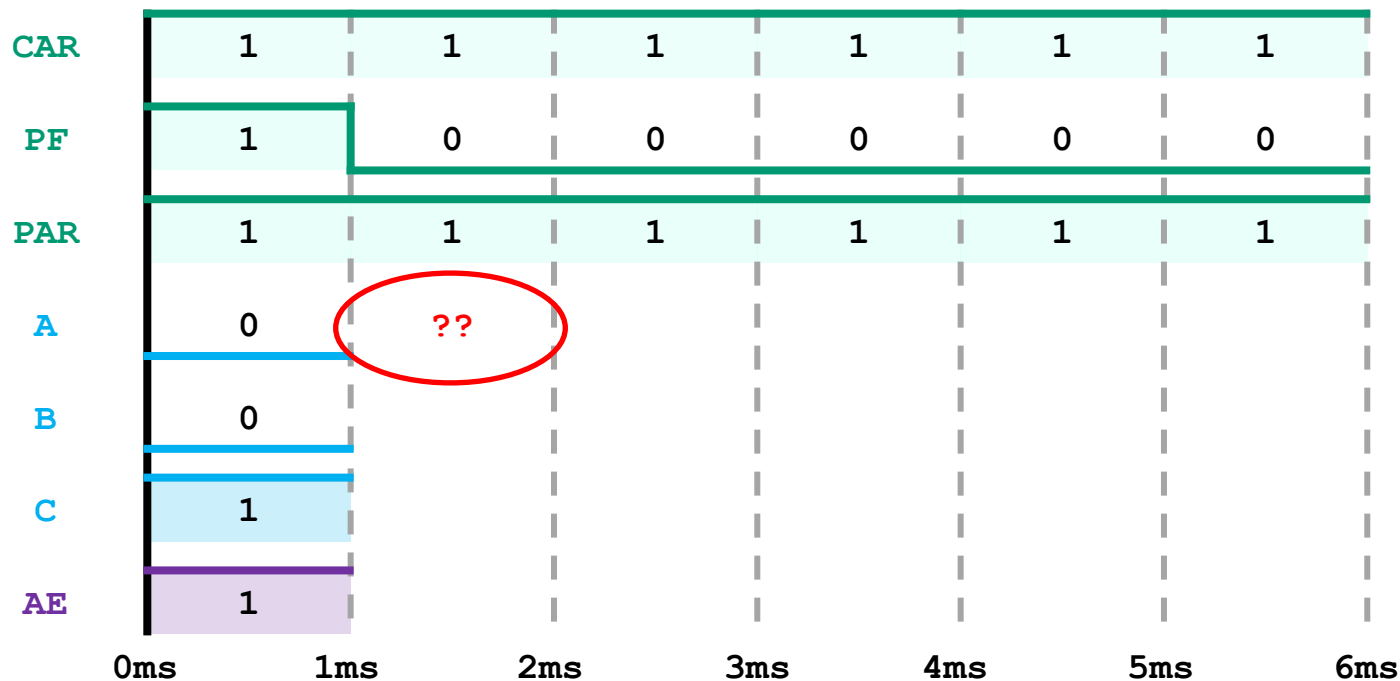
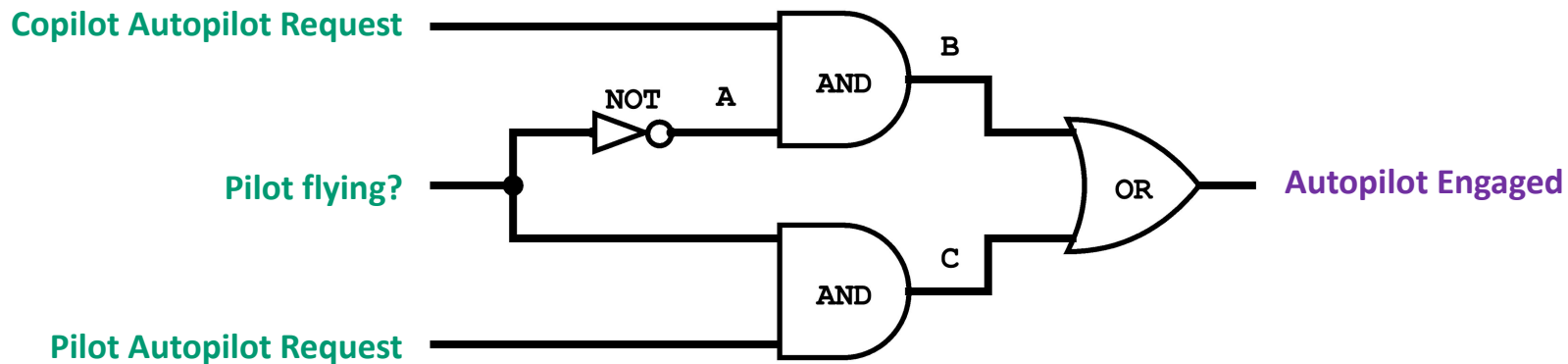
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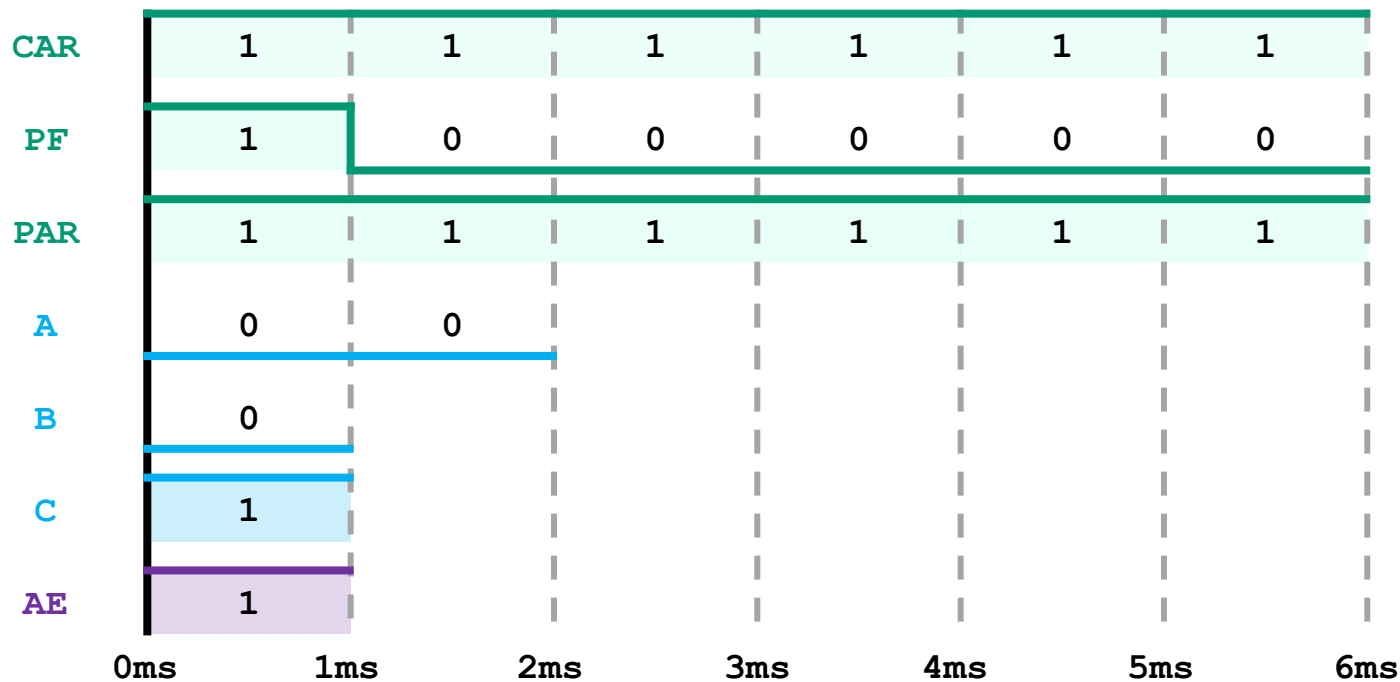
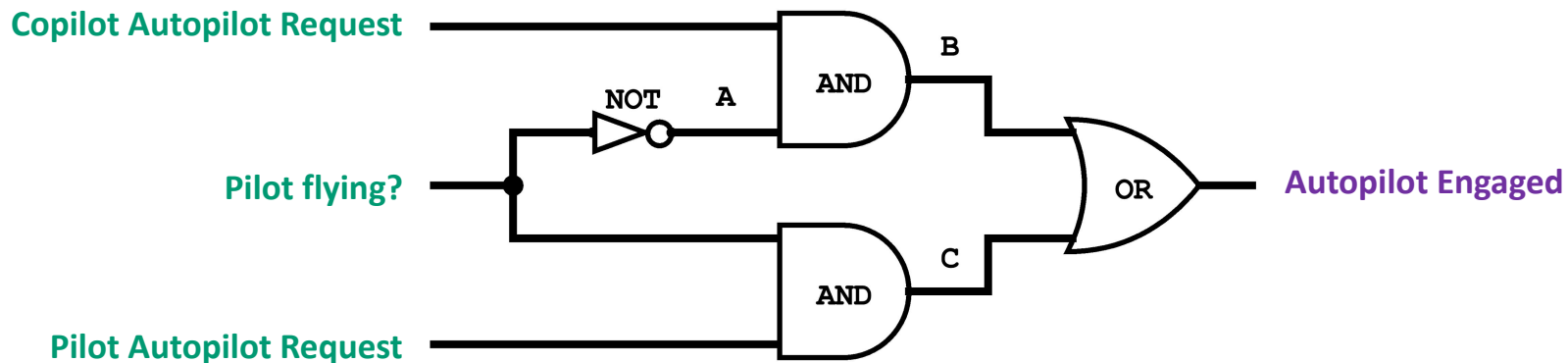
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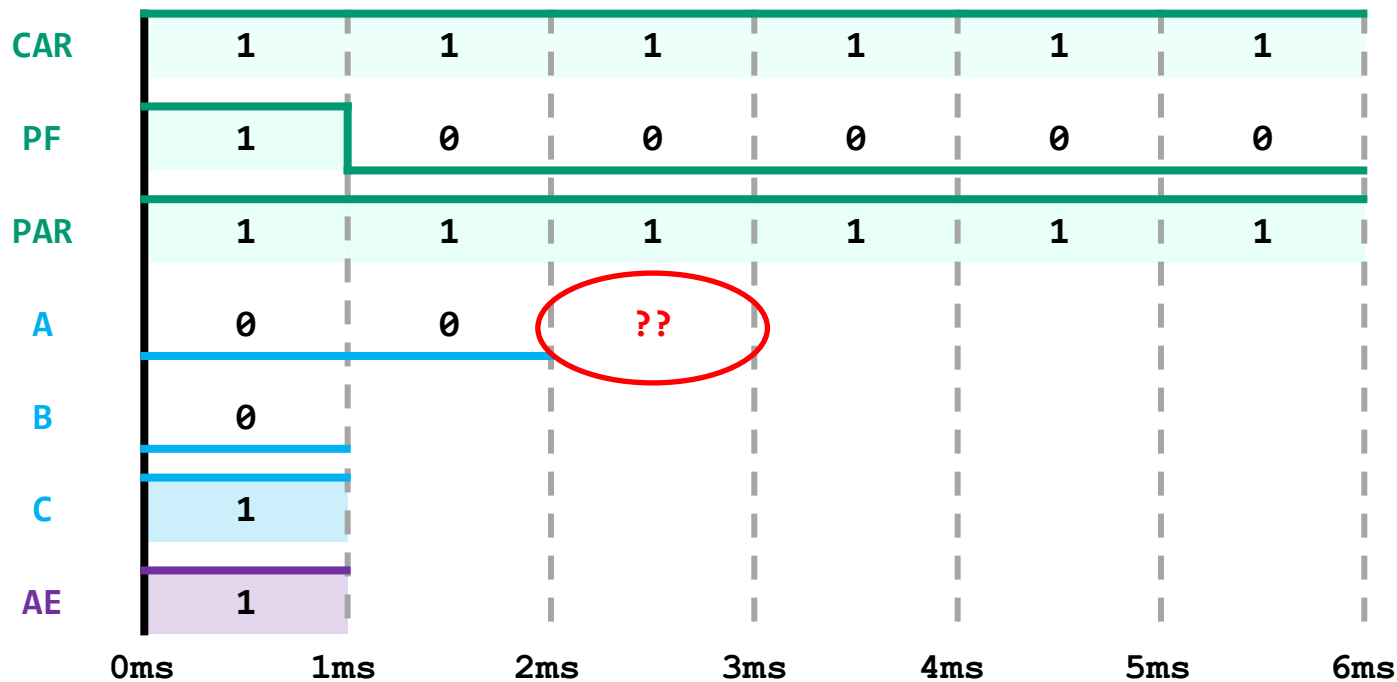
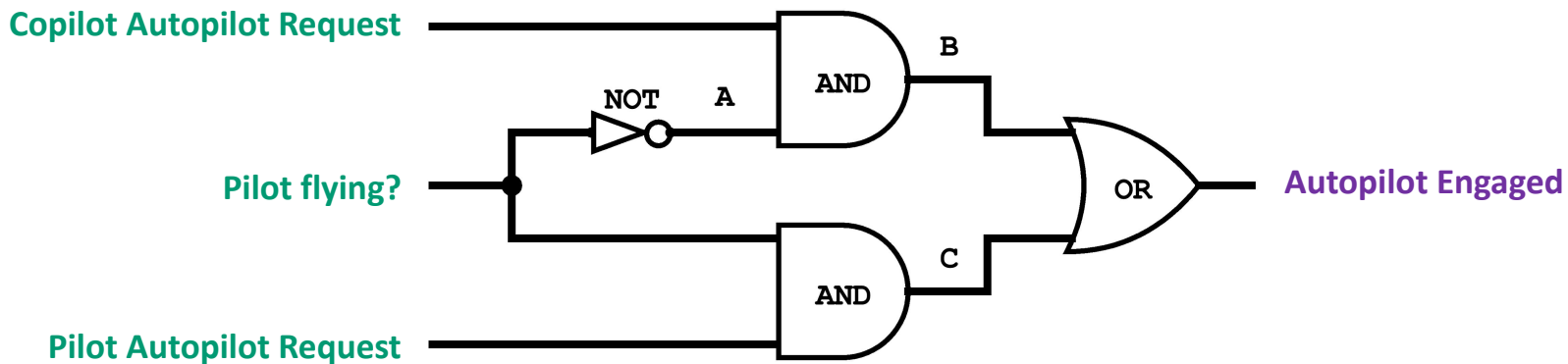
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Poll Everywhere

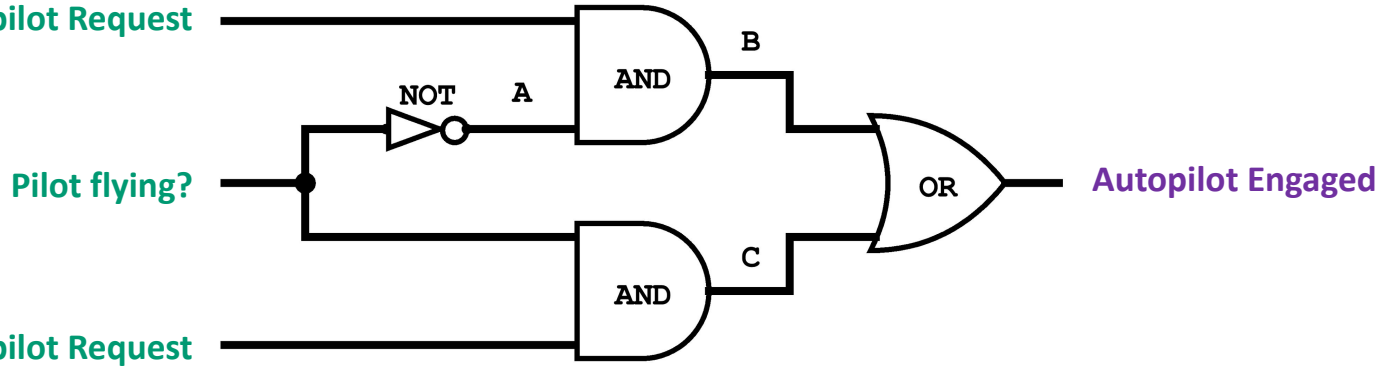
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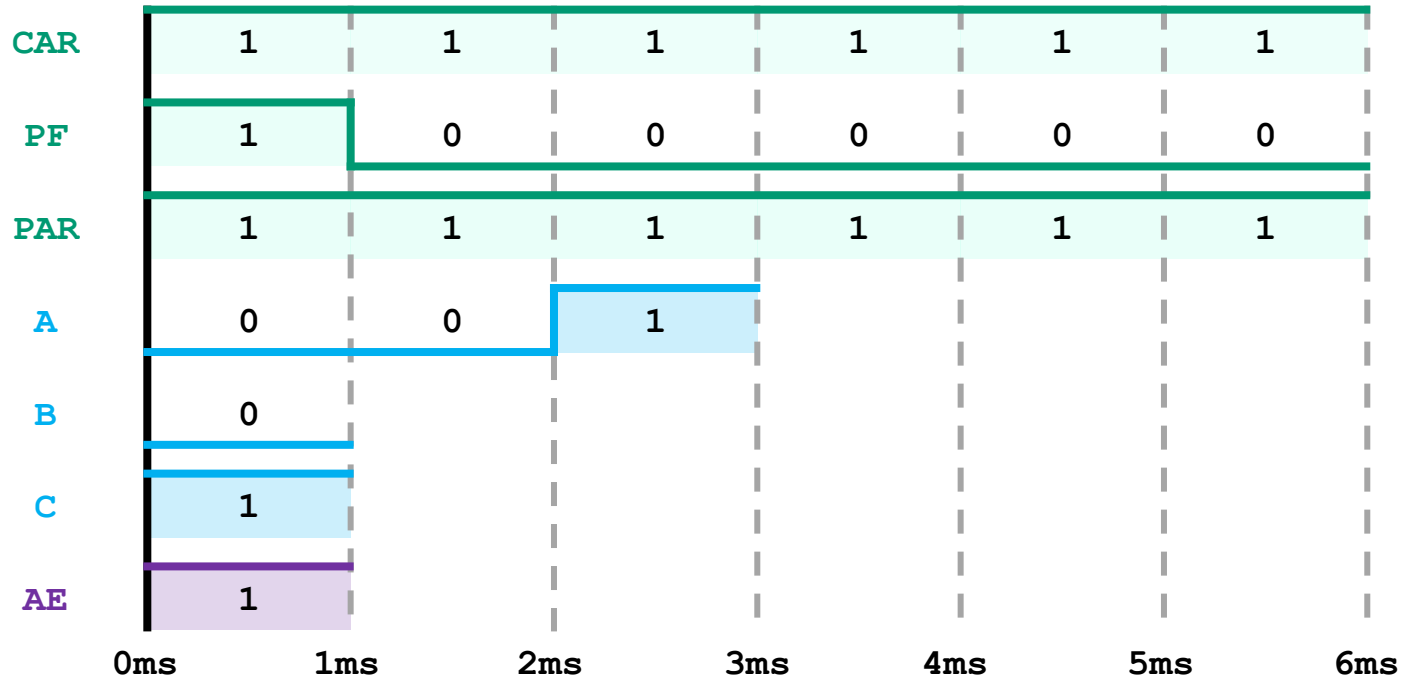
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Copilot Autopilot Request

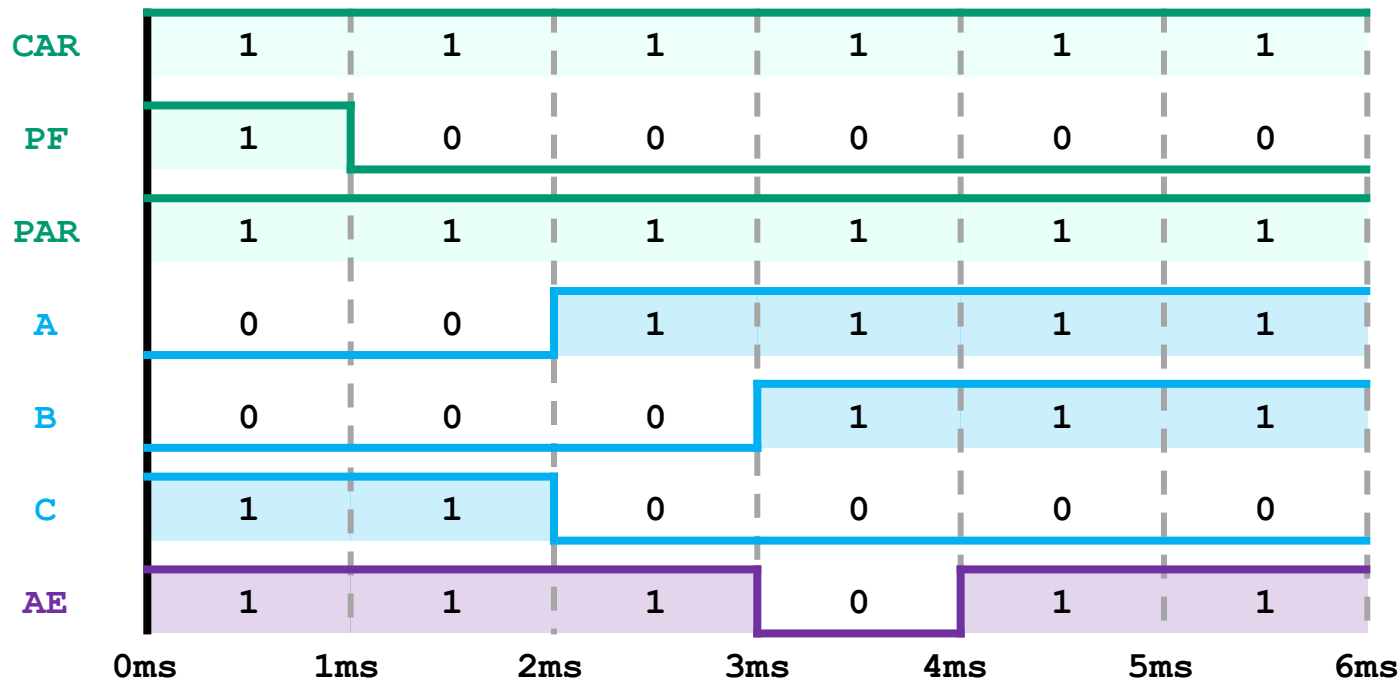
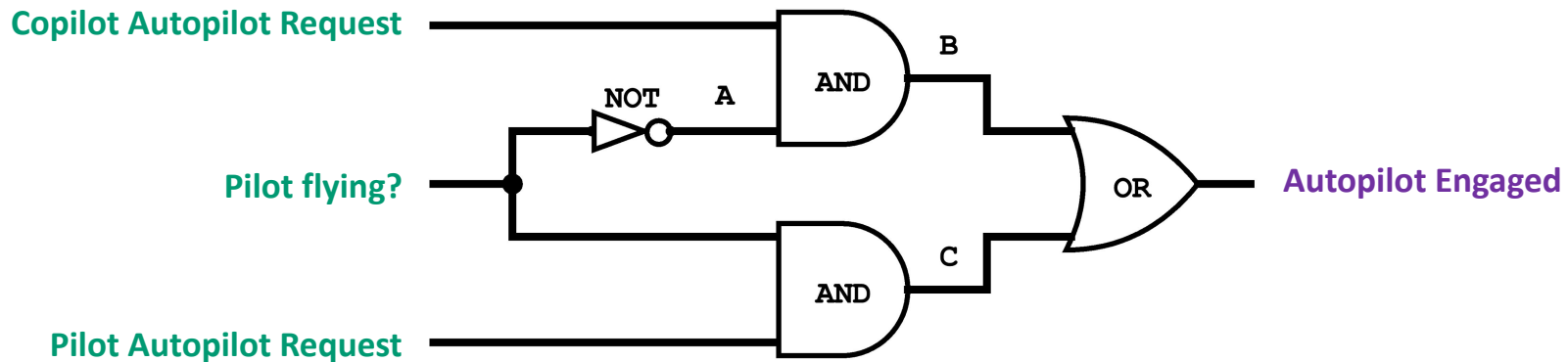


Pilot Autopilot Request



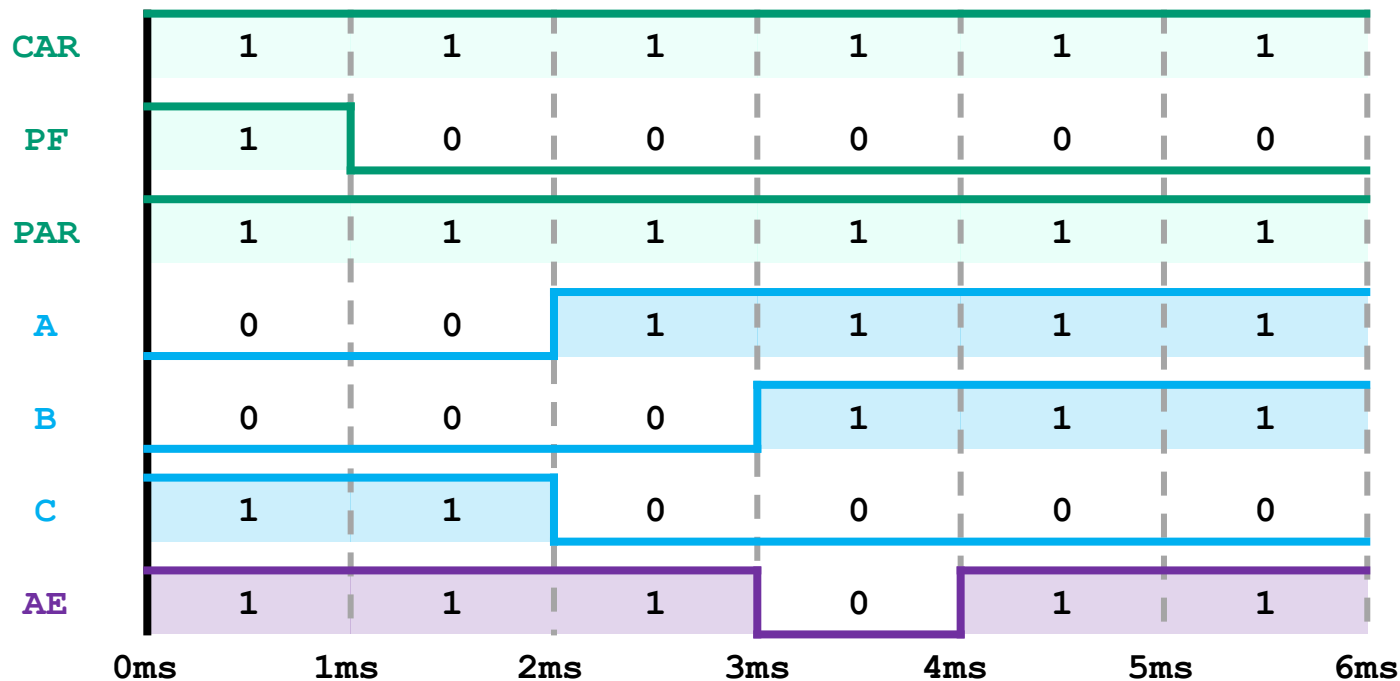
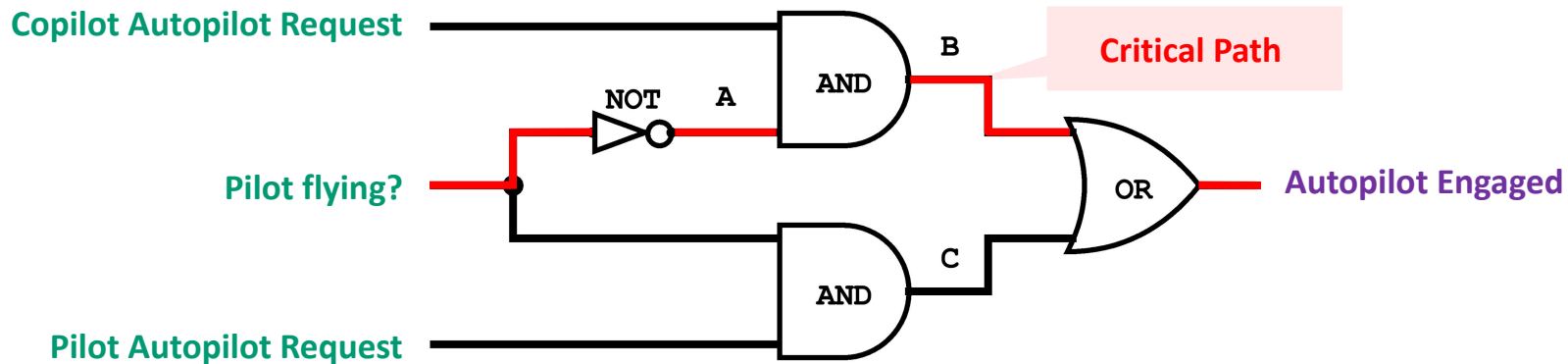
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Physical Timekeeping

- ❖ Hardware keeps track of time using an alternating signal
 - Creates the idea of **discrete time**: state changes only occur in discrete intervals, right when signal alternates

Physical
Time



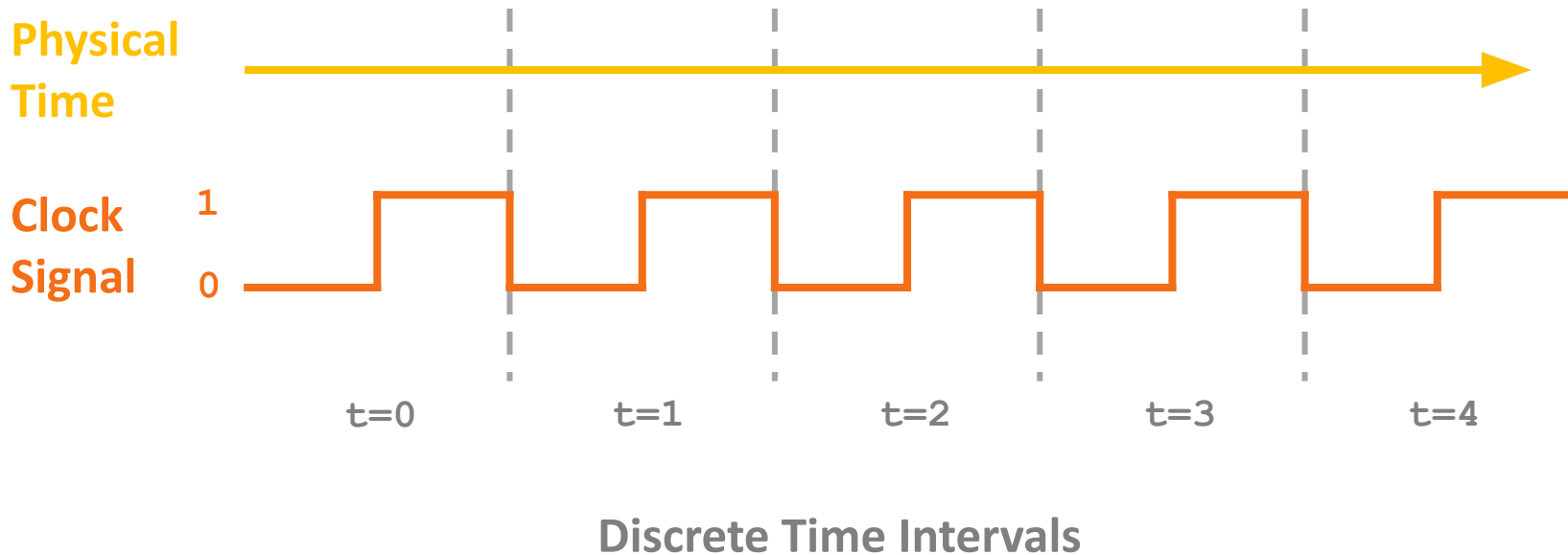
Clock
Signal

1
0

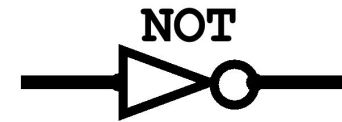


Physical Timekeeping

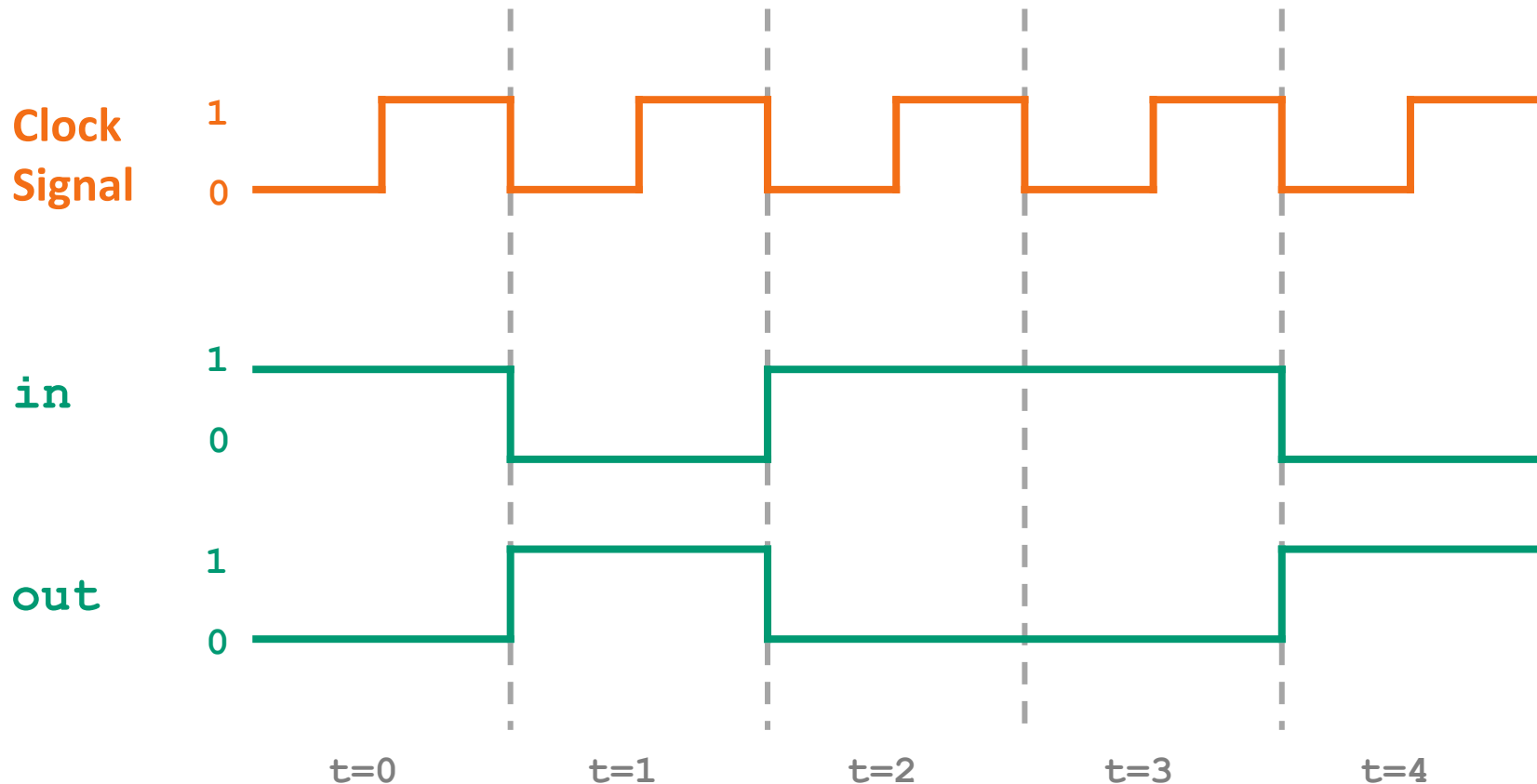
- ❖ Hardware keeps track of time using an alternating signal
 - Creates the idea of **discrete time**: state changes only occur in discrete intervals, right when signal alternates



Adding a Clock: Ideal

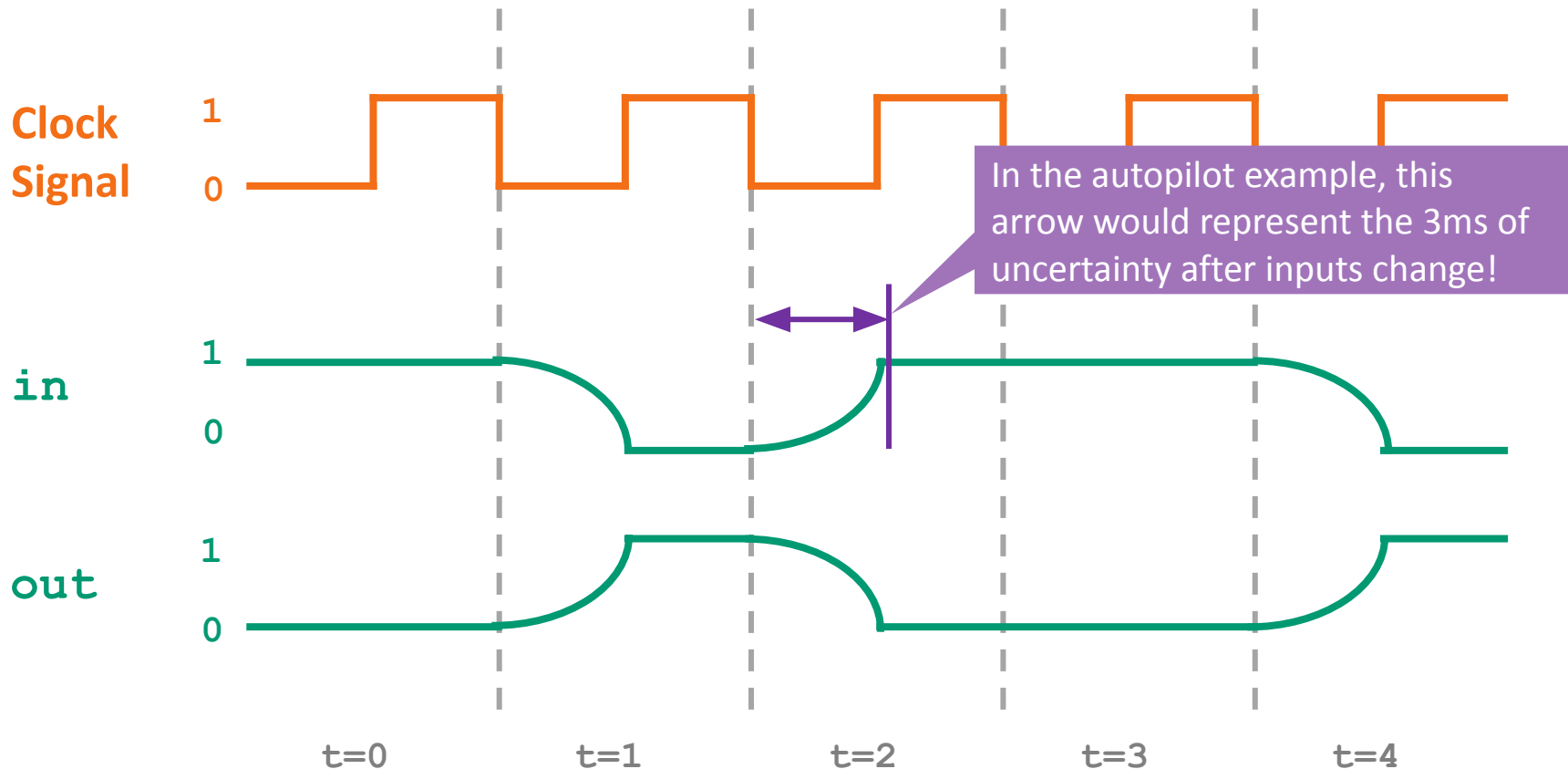


- ❖ We want this behavior from a simple, combinational Not gate:



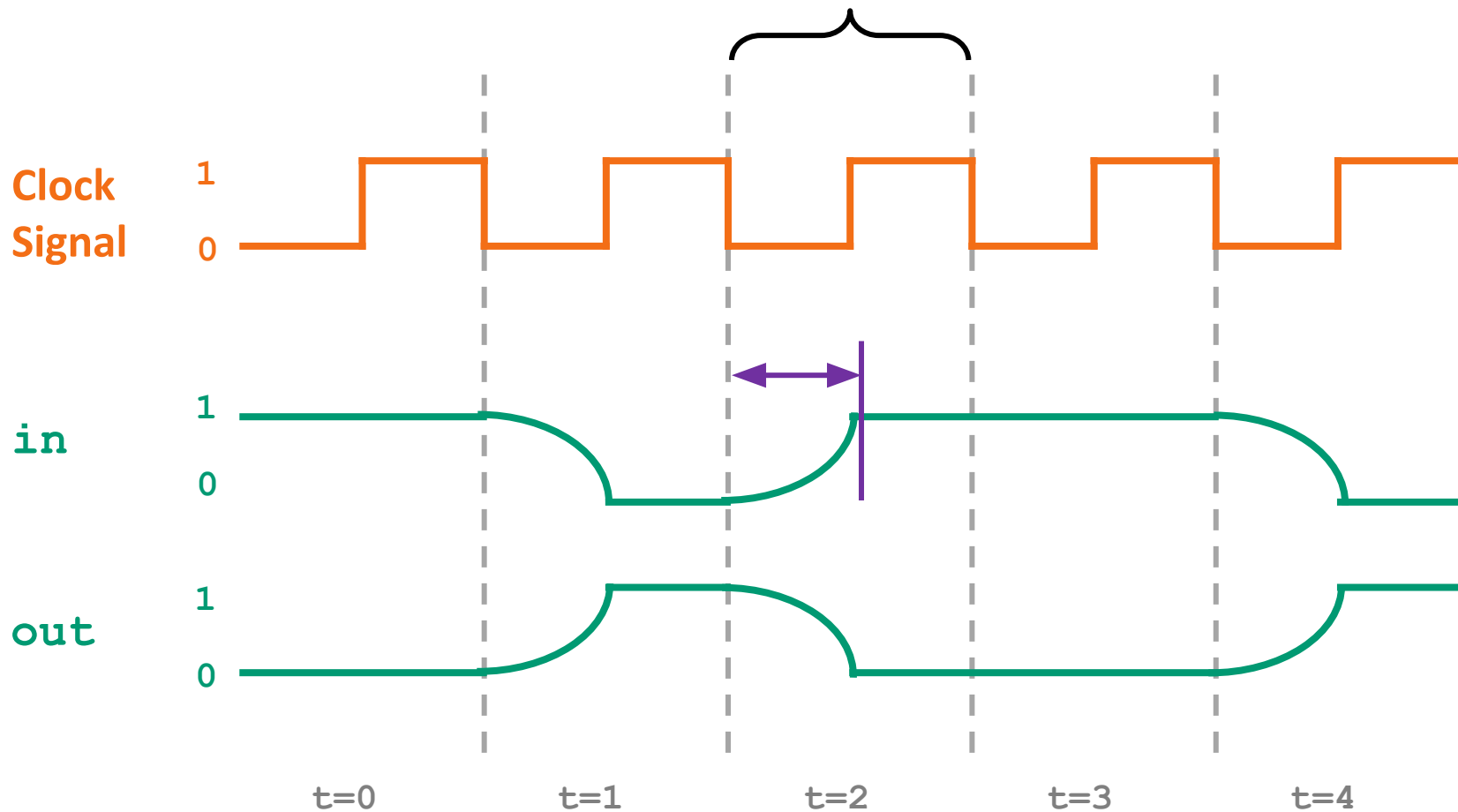
Adding a Clock: Reality

- ❖ Combinational logic may be incorrect for a period immediately after inputs change
 - **Computation delays** (logic gates) and **propagation delays** (wires)



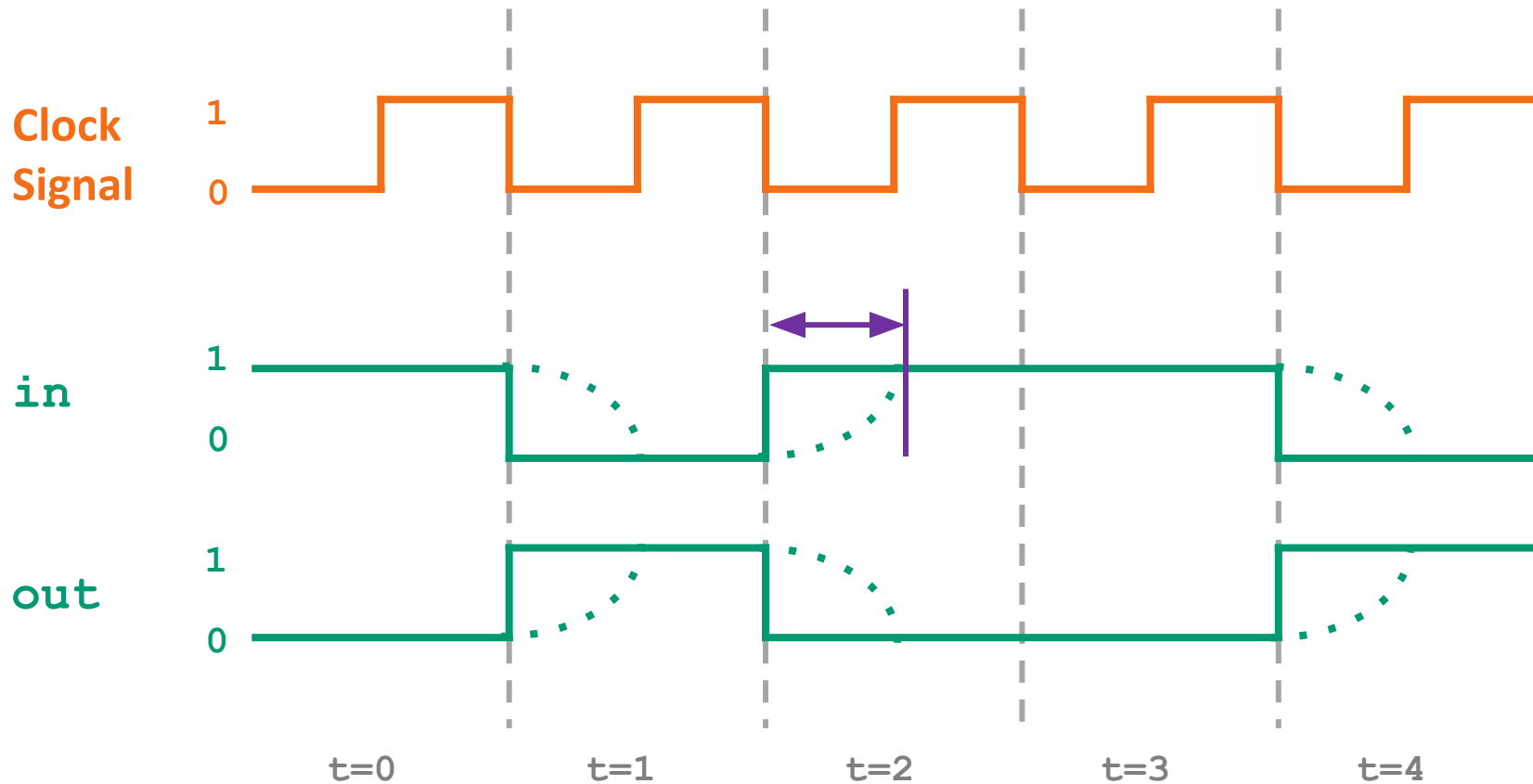
Adding a Clock: Clock Cycles

- ❖ Choose a clock cycle length slightly longer than the delays



Adding a Clock: Abstraction

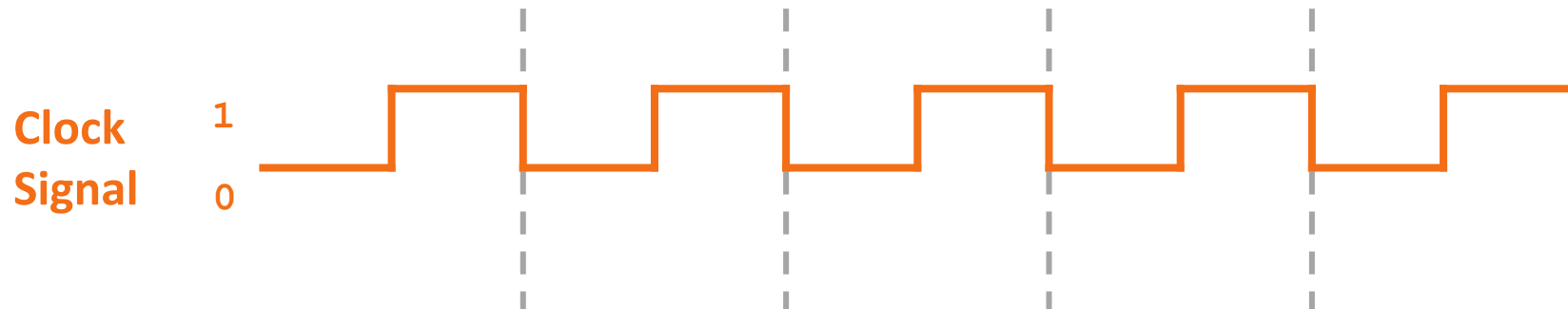
- ❖ If we use a long enough clock cycle, we can *pretend* that combinational chips (like Not) work instantly



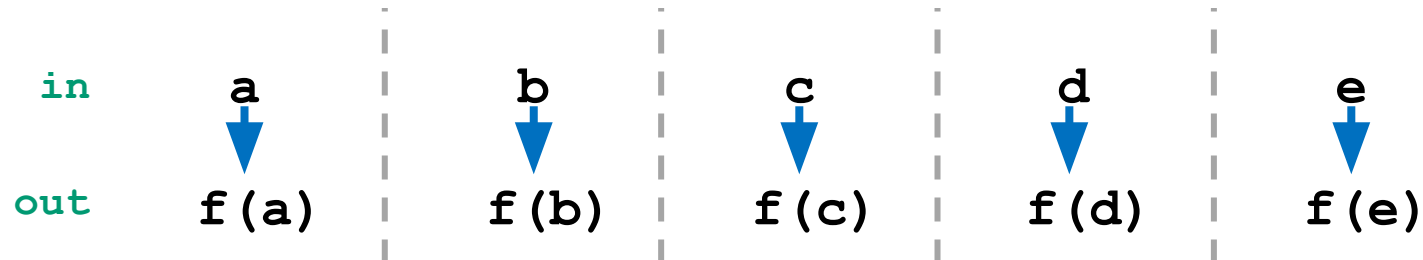
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- ❖ **Sequential Logic**
 - **Data Flip-Flip (DFF) implementation and examples**

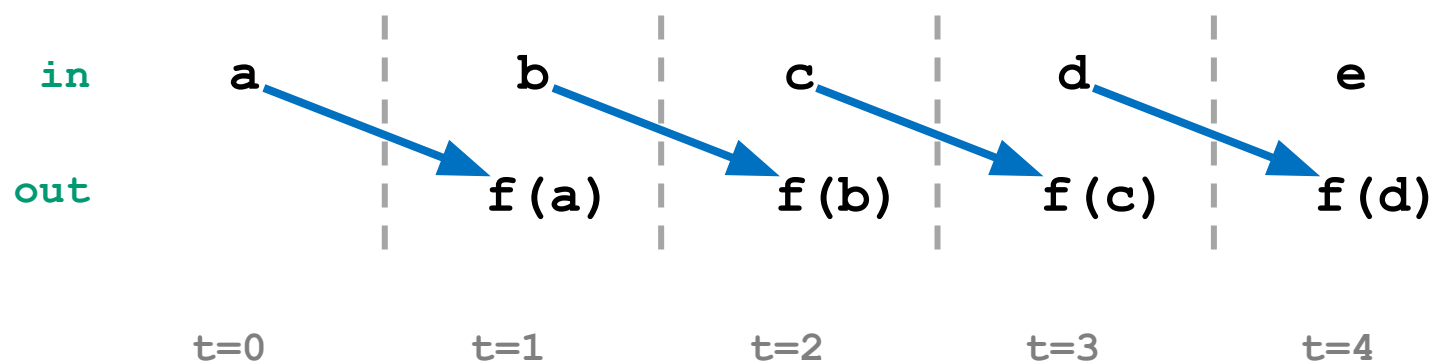
Combinational vs. Sequential Abstraction



Combinational: a function of the current inputs

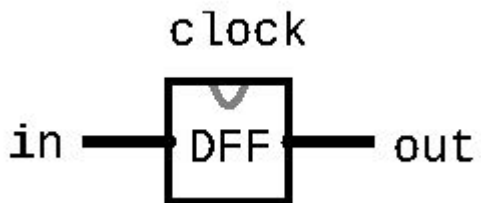


Sequential: a function of previous inputs (has "memory")



The Flip-Flop Gate

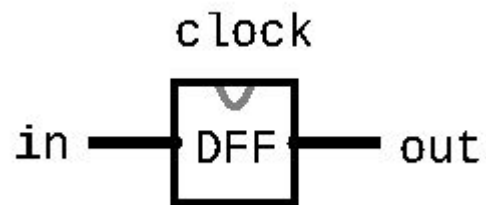
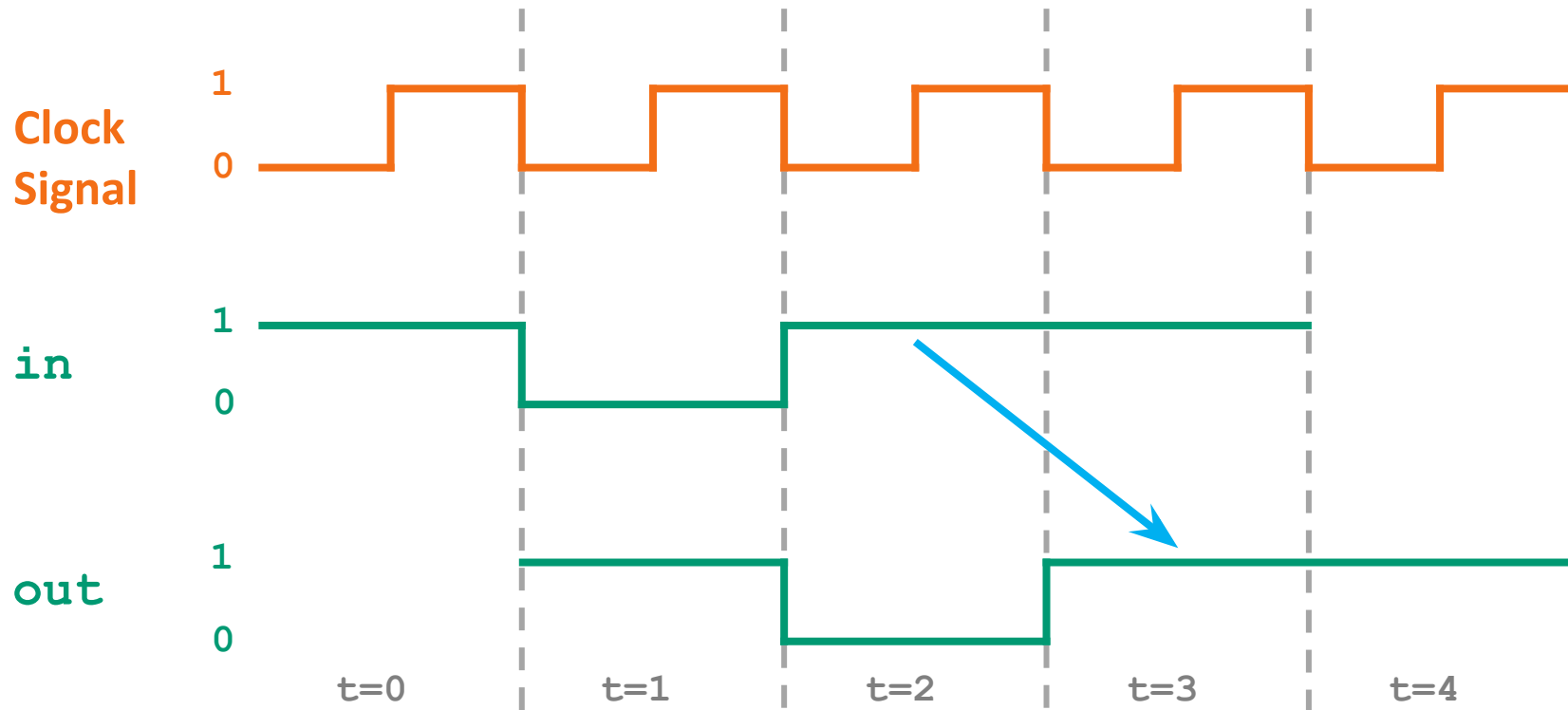
- ❖ Simplest state-keeping component
 - 1-bit input, 1-bit output
 - Wired to the clock signal
 - Always outputs its previous input: $\text{out}(t) = \text{in}(t-1)$
- ❖ Implementation: a gate that can flip between two stable states (remembering 0 vs. remembering 1)
 - Gates with this behavior are “Data Flip Flops” (DFFs)



Aside: Treating Flip-Flop as Primitive

- ❖ Disclaimer: CAN be made from Nand gates exclusively!
 - But requires wiring them together in a “messy” loop that the hardware simulator can't simulate and isn't very educational
- ❖ For simplicity, we will treat Flip-Flop as primitive in the projects
 - Just like Nand, you can use the built-in implementation

Flip-Flop Behavior



Sequential Chips

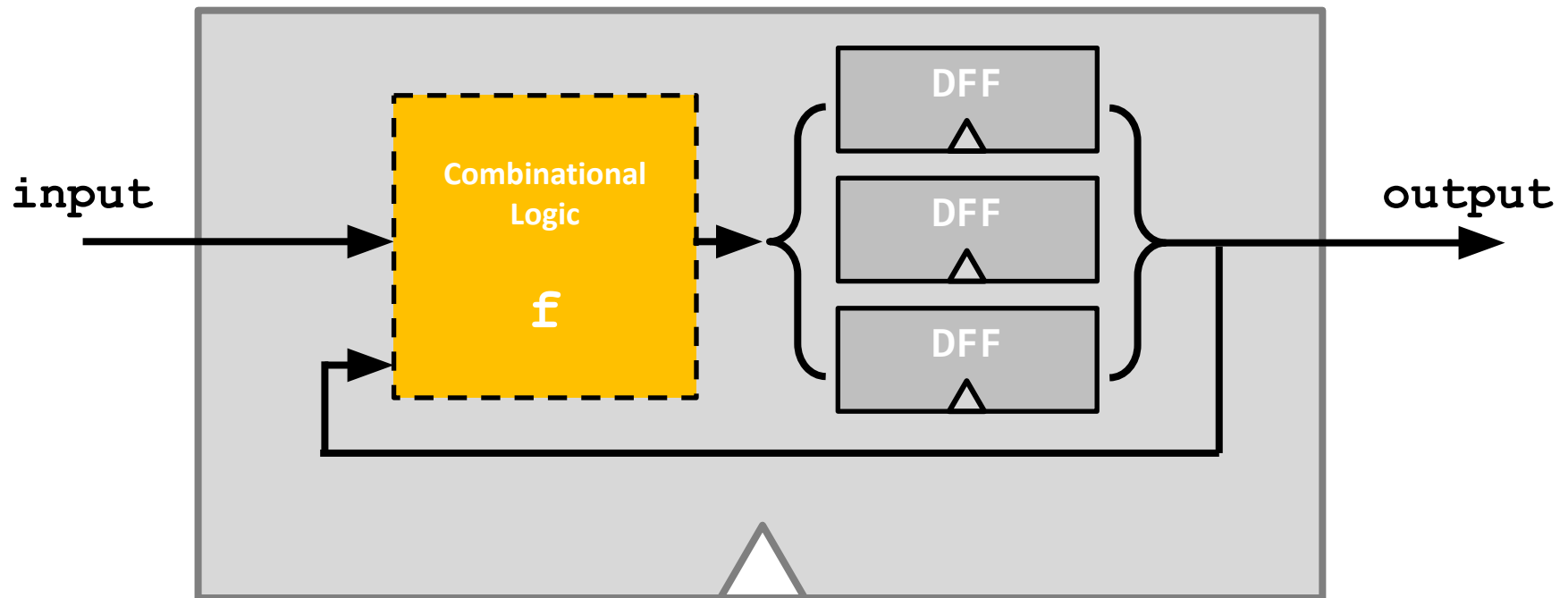
- ❖ A category of chips that utilize the clock signal, in addition to any combinational logic

- ❖ Capable of:
 - Maintaining state
 - Optionally, acting on that state & current inputs
 - Can incorporate combinational logic as well

- ❖ Constructed from:
 - DFFs
 - Combinational logic (which is entirely constructed from Nand)

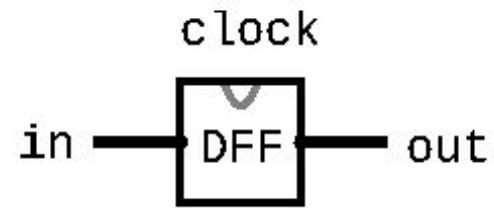
Sequential Chips

$$\text{output}(t) = f(\text{state}(t-1), \text{input}(t))$$



Flip-Flop: Time Series

❖ DFF Specification:



$$\text{out}(t) = \text{in}(t-1)$$

in	0	0	1	1	0	1	0	...
out	0	0	0	1	1	0	1	...
time	t=0	t=1	t=2	t=3	t=4	t=5	t=6	...

Example: $\text{out}(t=3) = \text{in}(t=2)$

DFF Example 1: Specification

- ❖ Example specification:

$$\text{out}(t) = \text{Xor}(a(t-1), b(t-1))$$

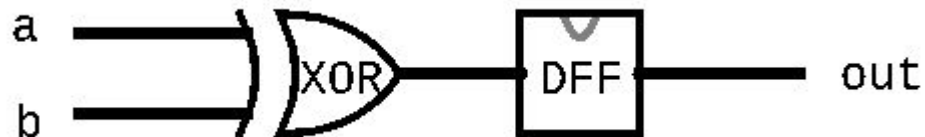
- ❖ Takes two inputs, a and b , and outputs the `XOR` of them
 - Note that out at time t is determined by a and b at time $t-1$
 - We will need to use a DFF!
- ❖ Exercise: Draw out the corresponding circuit diagram

DFF Example 1: Circuit Diagram

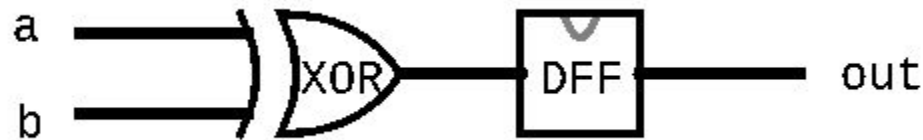
- ❖ Example specification:

$$\text{out}(t) = \text{Xor}(a(t-1), b(t-1))$$

- ❖ Circuit diagram:



DFF Example 1: HDL Implementation



```
CHIP Example1 {  
  IN a, b;  
  OUT out;
```

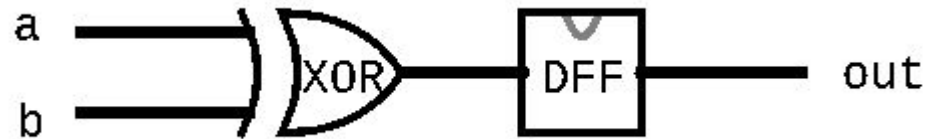
PARTS:

```
Xor(a=a, b=b, out=xorout);  
DFF(in=xorout, out=out);
```

```
}
```

DFF Example 1: Time Series

❖ Example specification:



$$\text{out}(t) = \text{Xor}(a(t-1), b(t-1))$$

a	0	0	1	1	1	0	0	...
b	0	1	0	1	1	1	0	...
out	0	0	1	1	0	0	1	...
time	t=0	t=1	t=2	t=3	t=4	t=5	t=6	...

Example: $\text{out}(t=3) = \text{Xor}(a(t=2), b(t=2))$

DFF Example 2: Specification

- ❖ Example specification:

$$\text{out}(t) = \text{Xor}(\text{out}(t-1), \text{in}(t-1))$$

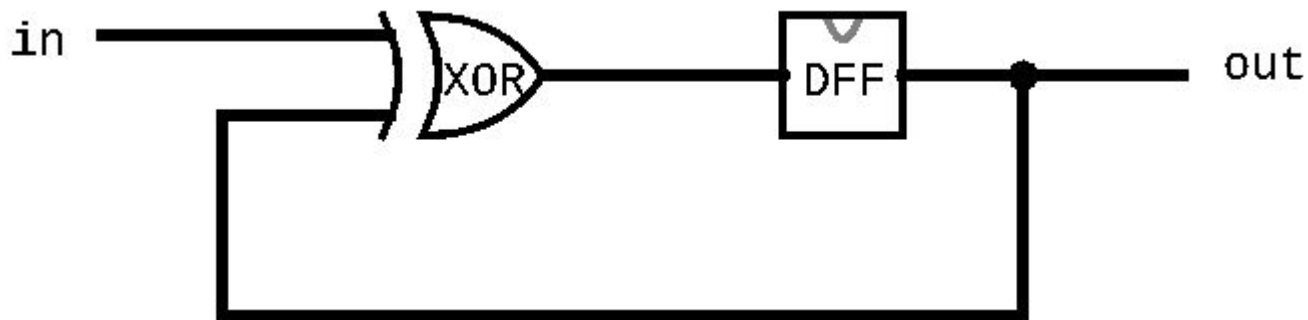
- ❖ Notice how the specification uses **out(t-1)** as an input for **out(t)**
 - Implies the necessity of circular wiring, separated by a DFF
- ❖ Exercise: Draw out the corresponding circuit diagram

DFF Example 2: Circuit Diagram

- ❖ Example specification:

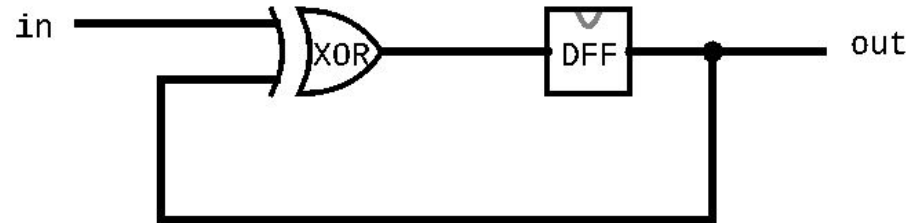
$$\text{out}(t) = \text{Xor}(\text{out}(t-1), \text{in}(t-1))$$

- ❖ Circuit diagram:



DFF Example 2: HDL Implementation

- ❖ Example specification:

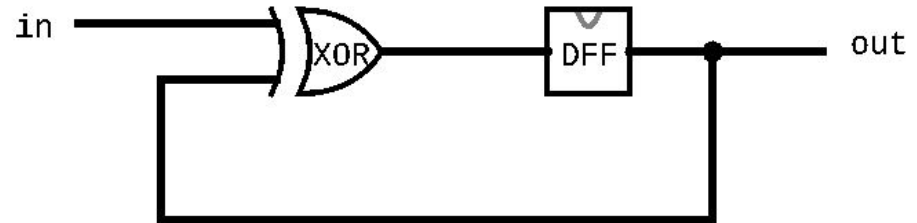


$$\text{out}(t) = \text{Xor}(\text{out}(t-1), \text{in}(t-1))$$

- ❖ Exercise: Write out the HDL Implementation

DFF Example 2: HDL Implementation

- ❖ Example specification:



$$\text{out}(t) = \text{Xor}(\text{out}(t-1), \text{in}(t-1))$$

- ❖ Exercise: Write out the HDL Implementation

```
CHIP Example2 {
```

```
  IN in;
```

```
  OUT out;
```

```
  PARTS:
```

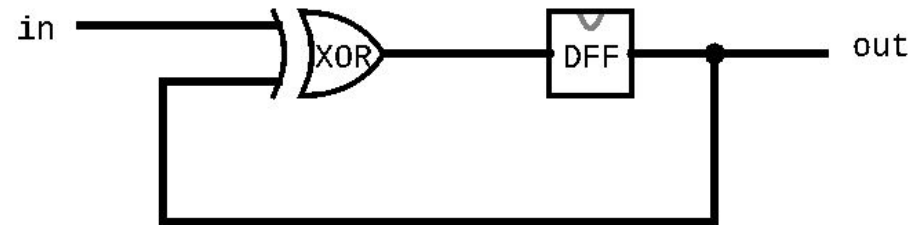
```
  Xor(a=in, b=prevout, out=xorout);
```

```
  DFF(in=xorout, out=prevout, out=out);
```

```
}
```

DFF Example 2: Time Series

❖ Example specification:



$$\text{out}(t) = \text{Xor}(\text{out}(t-1), \text{in}(t-1))$$

in	0	0	1	1	1	0	0	...
out	0	0	0	1	0	1	1	...
time	t=0	t=1	t=2	t=3	t=4	t=5	t=6	...

Example: $\text{out}(t=1) = \text{Xor}(\text{in}(t=0), \text{out}(t=0))$

DFF Example 3: Specification

- ❖ Example specification:

$$\text{out}(t) = \text{And}(\text{Not}(\text{out}(t-1)), \text{in}(t-1))$$

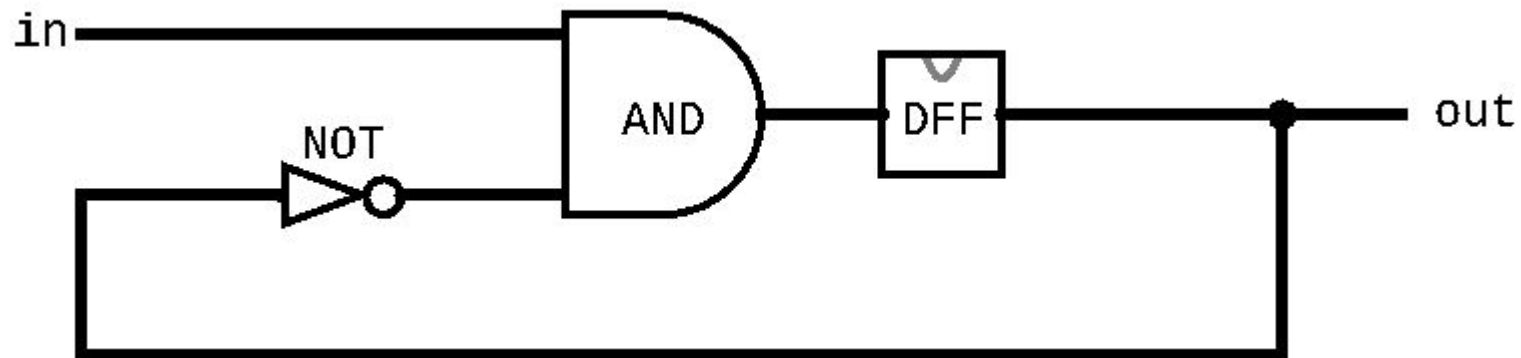
- ❖ Exercise: Draw out the corresponding circuit diagram

DFF Example 3: Circuit Diagram

- ❖ Example specification:

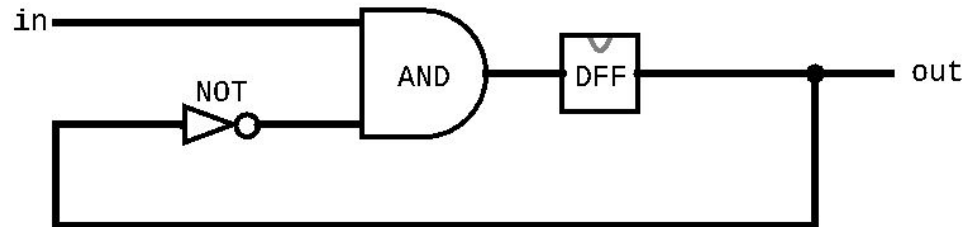
$$\text{out}(t) = \text{And}(\text{Not}(\text{out}(t-1)), \text{in}(t-1))$$

- ❖ Exercise: Draw out the corresponding circuit diagram



DFF Example 3: HDL Implementation

- ❖ Example specification:

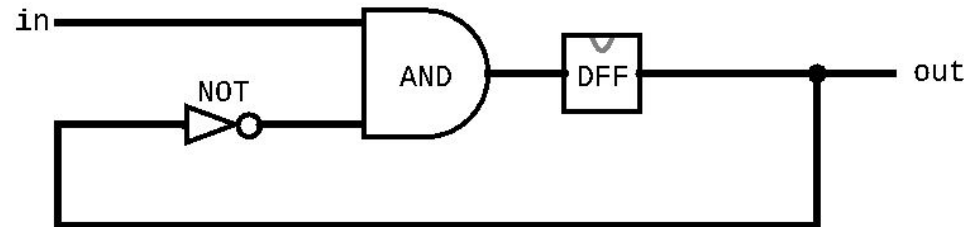


$$\text{out}(t) = \text{And}(\text{Not}(\text{out}(t-1)), \text{in}(t-1))$$

- ❖ Exercise: Write out the HDL Implementation

DFF Example 3: HDL Implementation

- ❖ Example specification:



$$\text{out}(t) = \text{And}(\text{Not}(\text{out}(t-1)), \text{in}(t-1))$$

- ❖ Exercise: Write out the HDL Implementation

```
CHIP Example3 {
```

```
    IN in;
```

```
    OUT out;
```

```
    PARTS:
```

```
    Not(in=prevout, out=notprevout);
```

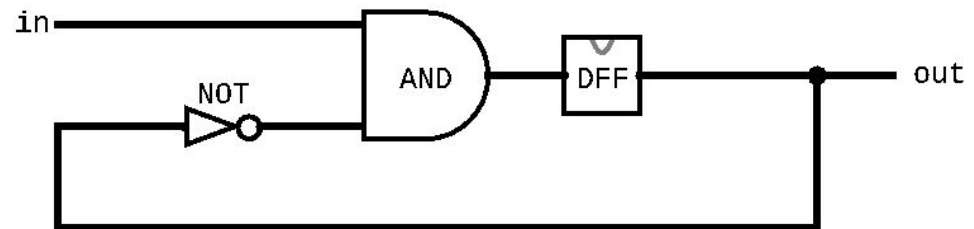
```
    And(a=in, b=notprevout, out=andout);
```

```
    DFF(in=andout, out=prevout, out=out);
```

```
}
```

DFF Example 3: Time Series

❖ Example specification:



$$\text{out}(t) = \text{And}(\text{Not}(\text{out}(t-1)), \text{in}(t-1))$$

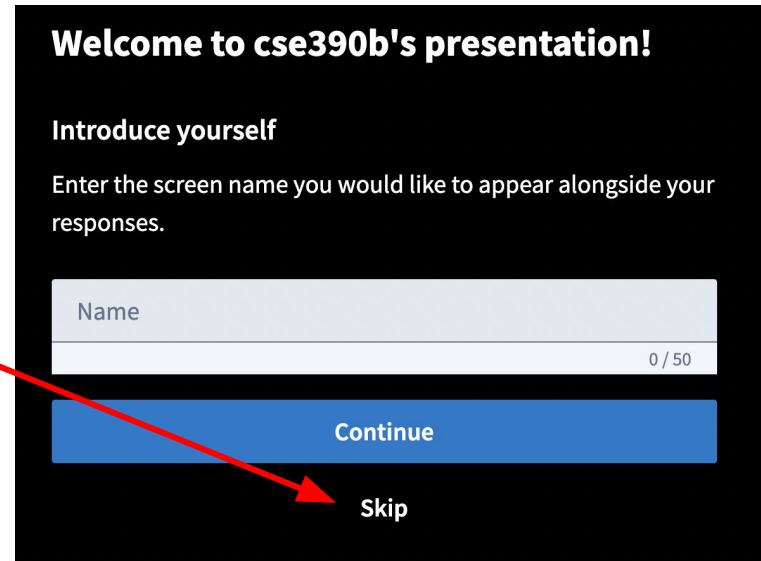
in	1	1	0	1	1	0	0	...
out	0	1	0	0	1	0	0	...
time	t=0	t=1	t=2	t=3	t=4	t=5	t=6	...

Example: $\text{out}(t=1) = \text{And}(\text{Not}(\text{out}(t=0)), \text{in}(t=0))$

 **Poll Everywhere**

Vote at <https://pollev.com/cse390b>

- ❖ **Are you available to attend at least one CSE 390B office hours? If not, what days and times would work better?**
- ❖ You can choose to respond anonymously by not entering your name (click “Skip”)



Welcome to cse390b's presentation!

Introduce yourself

Enter the screen name you would like to appear alongside your responses.

Name 0 / 50

Continue

Skip

Lecture 5 Reminders

- ❖ Project 1 grades released by tonight
 - Feedback can be viewed on Gradescope
- ❖ Project 2: Boolean Arithmetic, 24-Hour Time Audit
 - **Due on Thursday (1/20) at 11:59PM PST**
- ❖ Office Hours: Zoom links available via Canvas
 - Eric: Tuesdays and Thursdays, 3-4:00pm at CSE2 153
 - Leslie: Wednesdays, 4:30-5pm at CSE2 174
 - Audrey and Sean: Wednesdays, 1:30-2:30pm at CSE2 152
- ❖ Continue to ask your questions on the Ed board!