CSE 378 Autumn 1999

Machine Organization and Assembly Language Programming

Problem Set #6

Due: Thursday, November 18

This assignment is on pipelining. You should have read Chapter 6, Sections 1 through 6.

1. Exercises 6.2 and 6.4 (show RAW, WAR, and WAW dependencies) .
2. Exercise 6.9 (Pipeline structure and control), 6.11 and 6.12.
3. Exercises 6.19 and 6.20.
4. Assume you wanted to add the "instruction"

$$R_t \leftarrow R_t + Mem[R_s + offset]$$

   to the MIPS ISA. How would you encode the instruction? Why would it be hard to add this instruction to the MIPS pipeline? If you were asked to do it at all costs, how would you transform the pipeline (don't give all the details but give the salient ones such as number of stages, resources, impact on forwarding and hazard units etc.)? What implications, if any, would it have on latencies of individual instructions and throughput of the pipeline.
5. Exercise 6.28 (this is related to predicated execution, a feature found in some modern micros such as the Alpha 21064 family and Intel IA-64).