Multiprocessors

Whatever speed is achieveable with a uniprocessor (number of PCs = 1) it is possible to execute more instructions with a multiprocessor. The question becomes, can these extra instructions be applied usefully?

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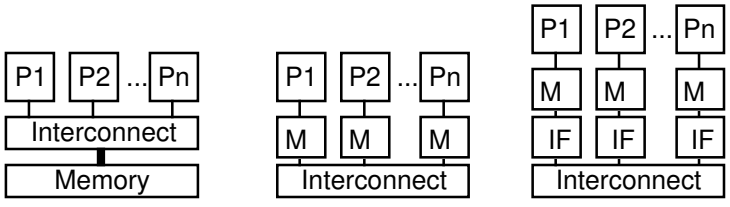
Critical Components

The critical issue in multiprocessor architecture is the arrangement and behavior of:

- Processors
- Memory(s)
- Interconnect



Shared Distributed Cluster

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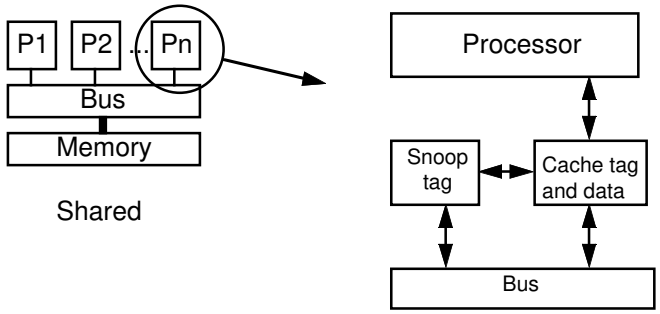
Symmetric Multiprocessors

An SMP architecture is a small set of processors connected to the memory bus, with snooping caches



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Snooping Protocols

- When reading a value, simply fetch it into the cache
- To keep the caches coherent, i.e. so that they are all seeing the same memory state, special actions take place on a store
  - Write invalidate -- writing processor causes all other processors to invalidate their cached copy
  - Write update -- the writing processor broadcasts the new copy to all processors

Snooping takes place on a cache block basis, so *false sharing* is a possibility

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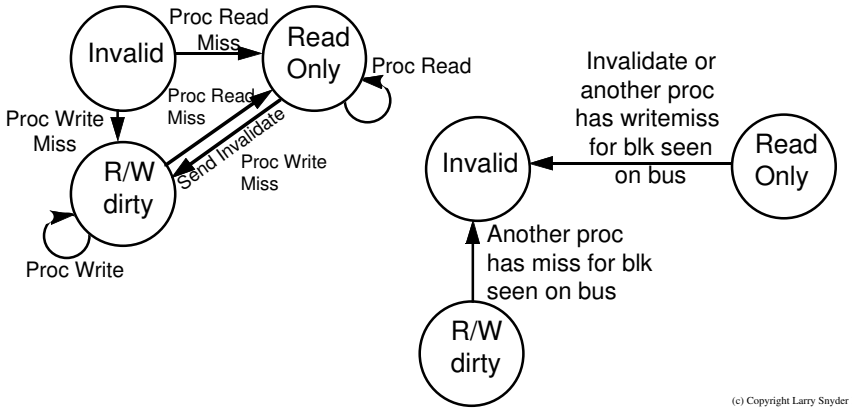
Cache Coherency Protocol

- The cache blocks can be in three states: read only, read/write, invalid



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Shared Memory Does Not Scale

- SMP allows several processors to reference same memory, but the bus is the bottleneck

Name	Procs	Proc	ClckMHz	CommBW
Compaq Proliant	4	PentiumPro	200	540MBs
DEC AlphaServer	12	Alpha21164	440	2150MBs
HP9000	4	PA8000	180	960MBs
IBMRS6000	8	PowerPC604	112	1800MBs
SGI Pow Challenge	36	MIPS R10000	195	1200MBs
Sun Enterprise	30	UltraSPARC	167	2600MBs

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