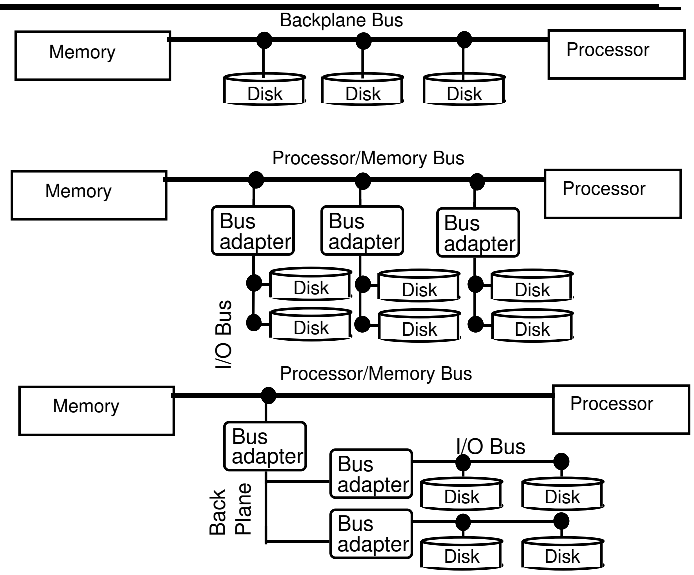
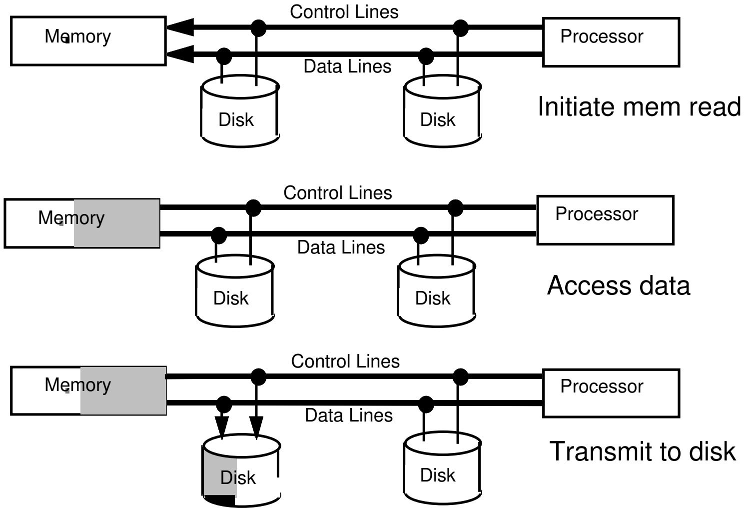
Networks and Buses

Buses and networks solve the problem of connecting components together.

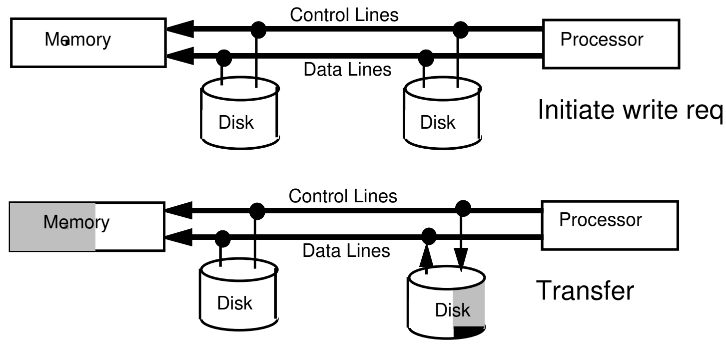
Alternatives



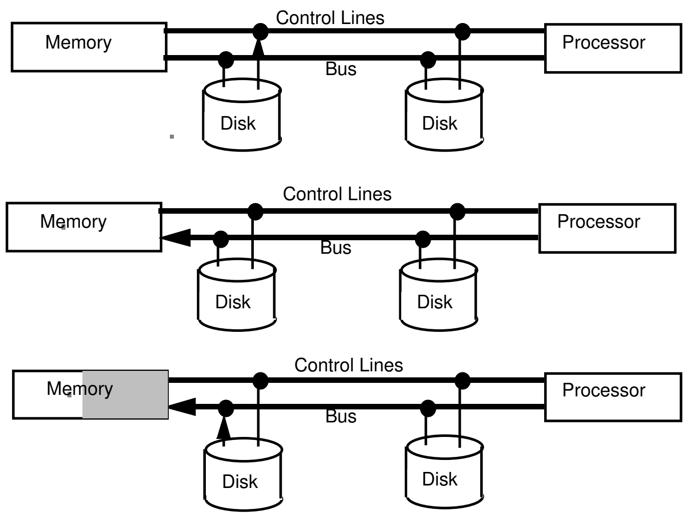
Output Operation



Input Operation

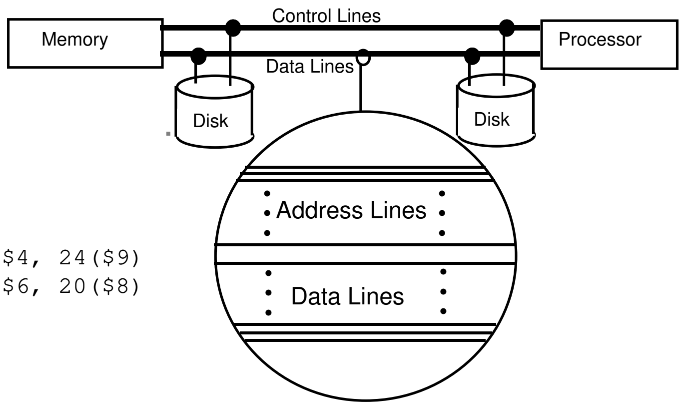


Single Bus Master



Memory Mapping

How does the processor refer to the memory and to peripheral devices over the same bus?




```
lw $4, 24($9)
sw $6, 20($8)
```

Bus Arbitration

- Deciding who will use a multimaster bus
- Goals: Prioritization and Fairness
- Four different schemes:
  - Daisy chaining
  - Centeral Master (PCI)
  - Distributed Self Selection (NuBus)
  - Distributed Arbitration by Collision Detection (Ethernet)

Transfering Data

Three techniques --

- Polling -- processor checks periodically
  - Ideal for low bandwidth devices, e.g. mouse
  - Impractical for fast devices
  - Penalized when no activity
- Interrupt Driven -- processor initiates, then is interrupted
  - Ideal for occasional use, faster devices, e.g. floopy
  - Impractical for very fast devices
- Direct Memory Access -- offload task to special controller
  - Ideal for disks
  - Relies on processor caching

Direct Memory Access

- Type of addressing --

  Physical addressing: Cannot cross page boundary due to non-contiguous allocation

  Virtual addressing: Requires translation

    Include a small address map with setup

    Chain pages together

- Coherency

  Data transfer to memory can differ with cache contents

    Route all memory accesses through cache

    Let software invalidate/flush cache

    Allow hardware to invalidate/flush cache