1. Assume the "usual" 5 step pipeline design, give a longest instruction sequence illustrating "data hazards".
2. How is a data hazard detected in hardware? Explain.
3. How can data hazards be reduced or eliminated in hardware? Explain.
4. What are the benefits/liabilities of solving data hazards in software?
5. What is a branch hazard? What are the options for handling it?
6. I/O device interrupts are handled more easily in a pipeline than arithmetic exceptions, e.g. overflow, because ...
7. What are temporal and spacial locality? Why are they so important?
8. In a cache what is the tag?
9. Consider a tight loop of 8 instructions that is executed 2^20 times, and containing a data hazard. Suppose there is an 8 word direct-mapped I-cache. What is the performance cost for this program of handling data hazards in software, assuming a miss penalty of 10 instruction times.
10. Writing to a cache is somewhat different depending on whether the cache is one word or several words wide. Explain the difference.
11. Miss Rate is not the star of a western novel, but ...
12. Caches have width and depth ... which helps temporal locality and which helps spacial locality?
13. What is the difference between early restart and requested word first?
14. Given a machine with a 15 cycle miss penalty, and a program with a 4% I-miss rate, a 8% D-miss rate, and 25% of the instructions reference D-memory, how much faster is the machine if the clock rate is doubled, given that CPI=3.
15. Give the steps in computing a physical address from a virtual address.
16. What does a page table contain?
17. Argue that LRU is unrealistic by explaining what would be required to implement it in the context of paging. Hint: Add a word to each page table entry to be a time stamp.
18. The opposite of write through is ... How does it work?
19. Why add page table bits, e.g. dirty bits, to the TLB?
20. Draw the schematic for an a 32-bit ALU with AND, OR, ADD, SUB, SLT.
21. On a page fault, how does the OS know what location caused the fault?
22. The book reports typical TLB miss rates .01%-1%. Why so low?
23. The opposite of direct mapped is ... Give an example where its used.
24. Will a 2-way or 4-way s. a. cache "conflict miss" less?
25. MIPS has 3 instruction formats and 5 addressing modes. What are they?
26. Explain polling, interrupt driven and DMA memory transfer methods.
27 From Track X, Sector Y a disk can reach what location fastest?
28. Explain memory-mapped I/O. Why pick it over custom I/O inst.s?
29. How many bits is the significand field for IEEE 64-bit floating point?
30. Using Figure 5.29, label the green control lines with the values they must have to implement (a) subi, (b) lw, (c) sw, (d) beq (e) jal.
31. Explain the difference between multicycle and pipeline datapaths.
32. Describe the contents of the ID/EX pipeline register.
33. What is the strangest term used in computer architecture?