Control and Exceptions

Finite-state machines are the most common implementation of the control logic for a machine. In CISC machines microcode extends the programming concept to implementing the instructions themselves.

Exceptions complicate the control slightly, but they are off the critical path.

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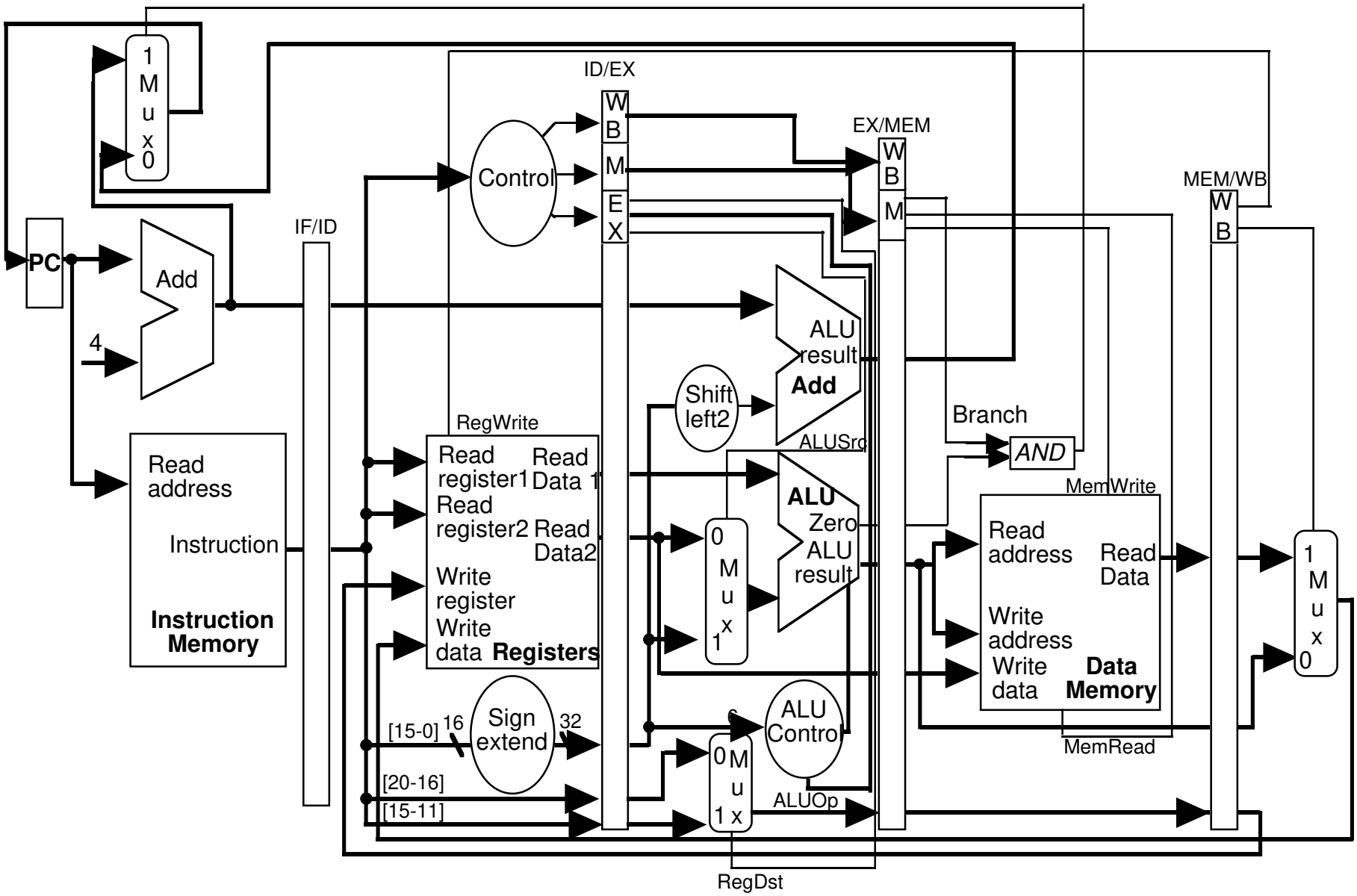
Datapath



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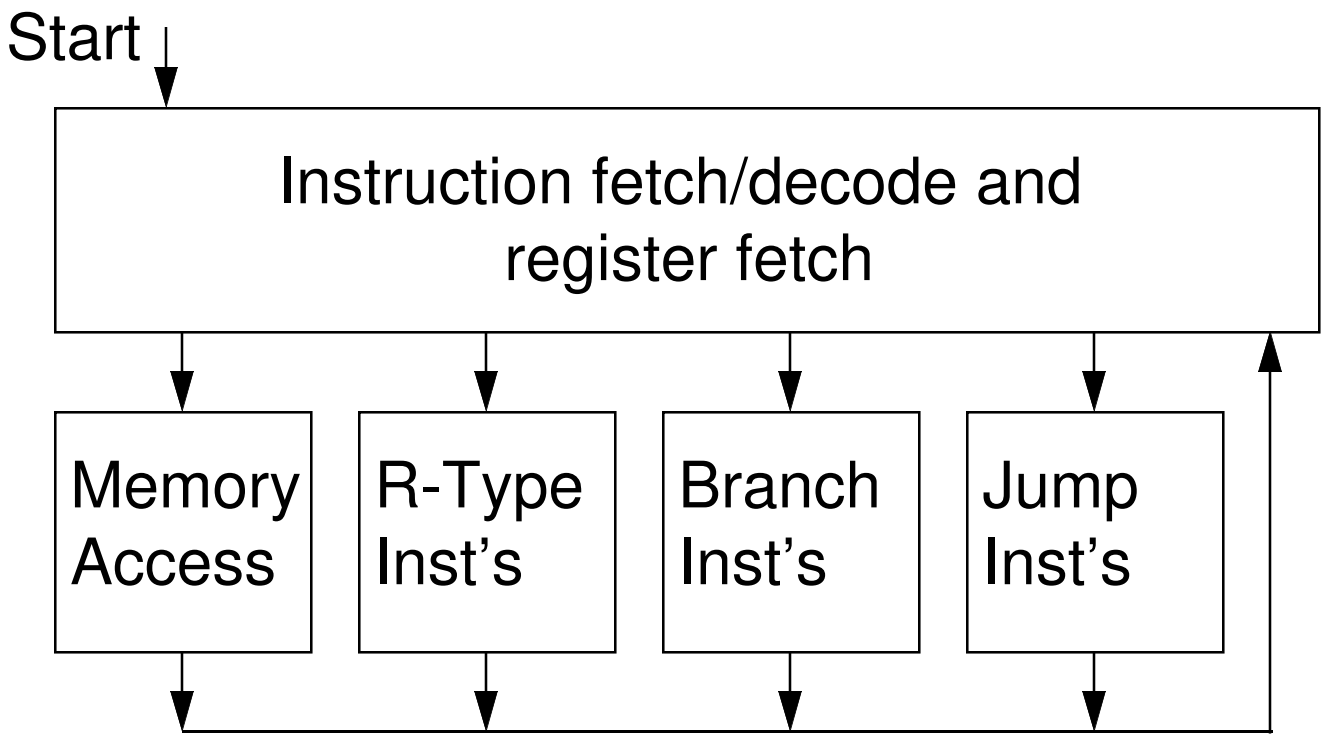
Finite State Control Overview

Goal: To stage the five steps of the execution



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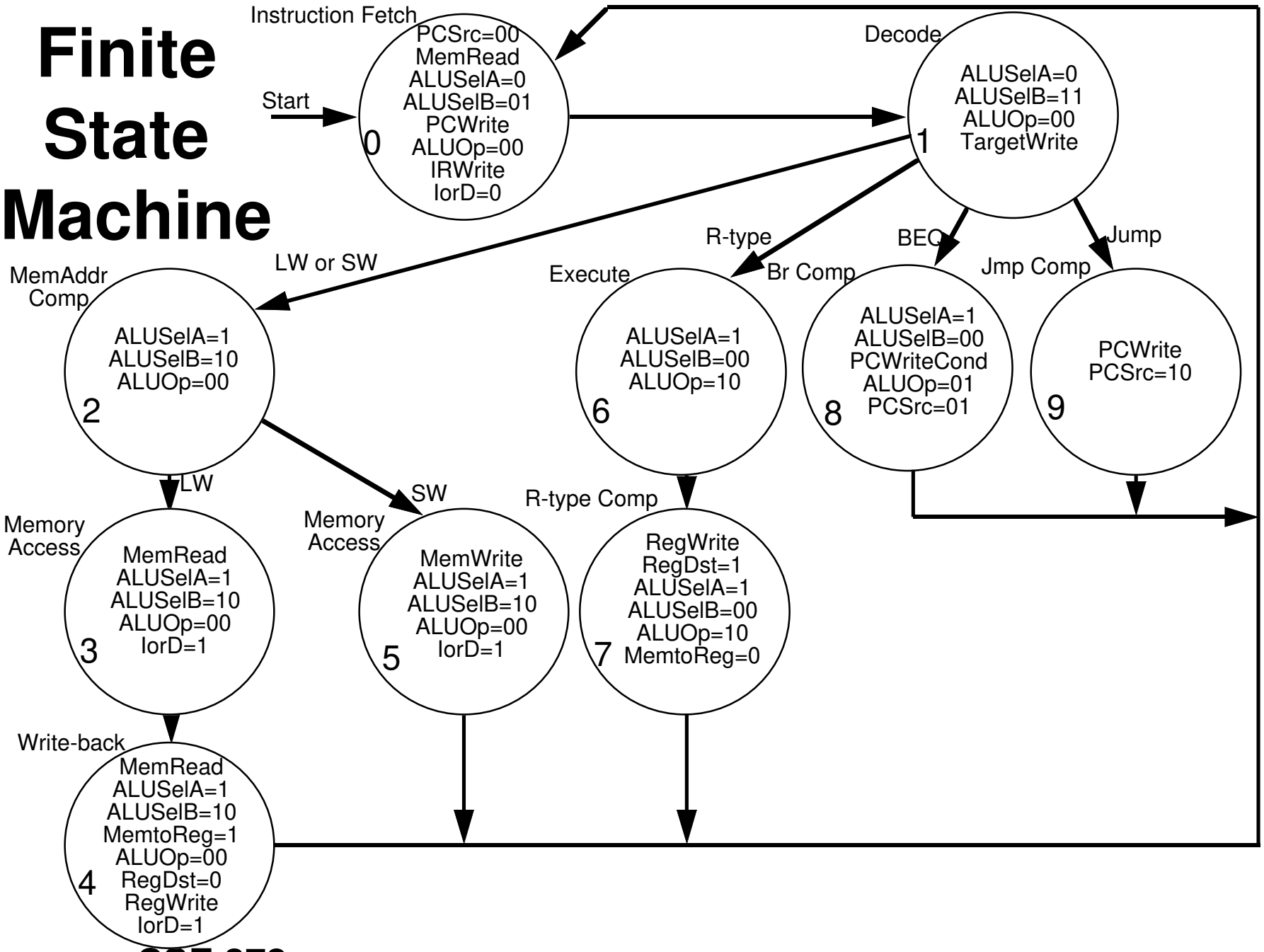
Finite State Machine



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Exceptions/Interrupts

- Exception / Interrupt vocabulary inconsistent
    - Exception -- unexpected change of control flow
    - Interrupt -- external notification of an event
- Examples: I/O Device, Invoke OS, Overflow, Undefined Instruction, Parity Error
- Knowing cause and location is critical
    - Save cause in special register
    - Vector into OS based on cause
- Define EPC and Cause Register
- Postulate EPC Write, CauseWrite, IntCause
- Agree OS exception handling is 40000000

Vectored Intrpts
Undef. Inst C0000000
Overflow C0000020

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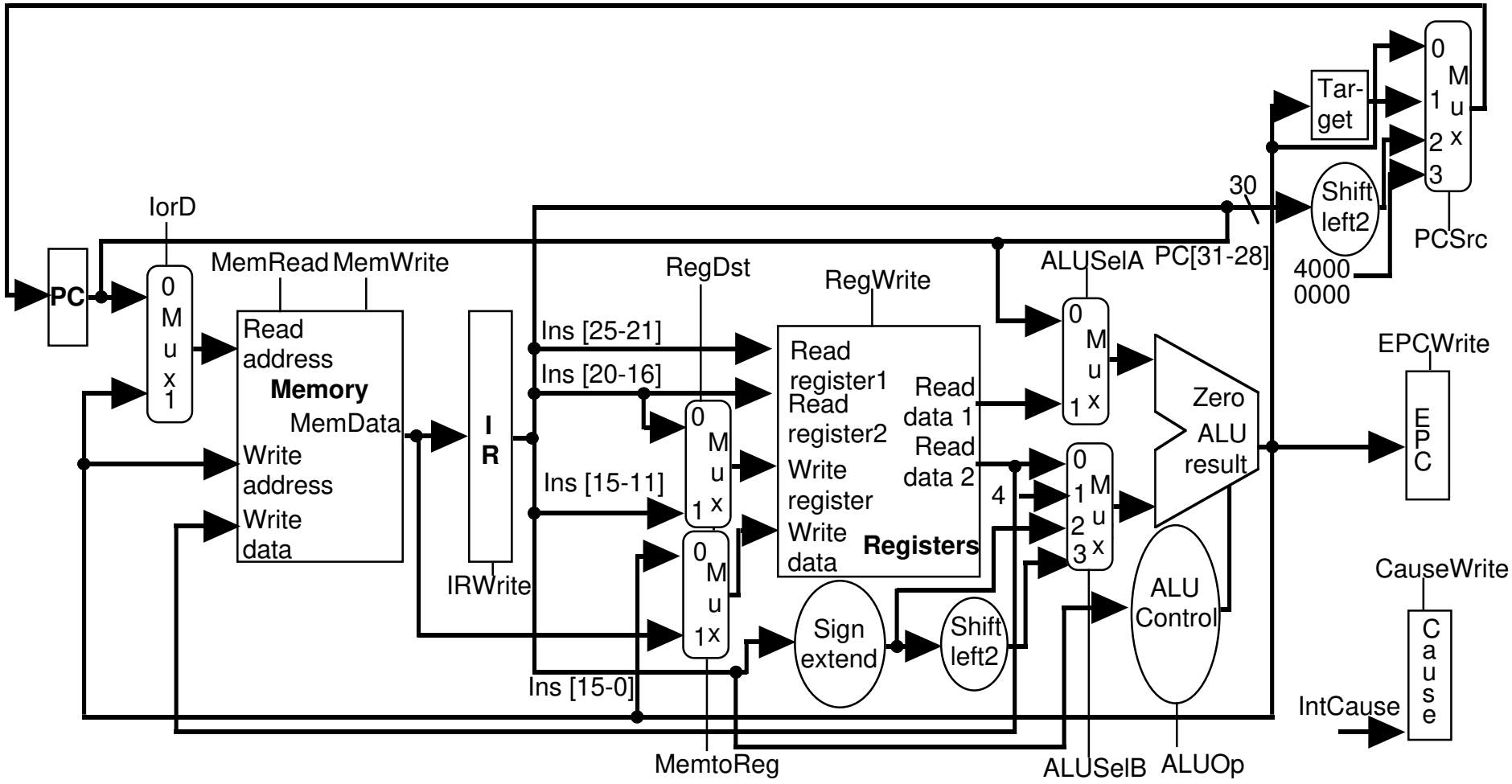
Handling Exceptions



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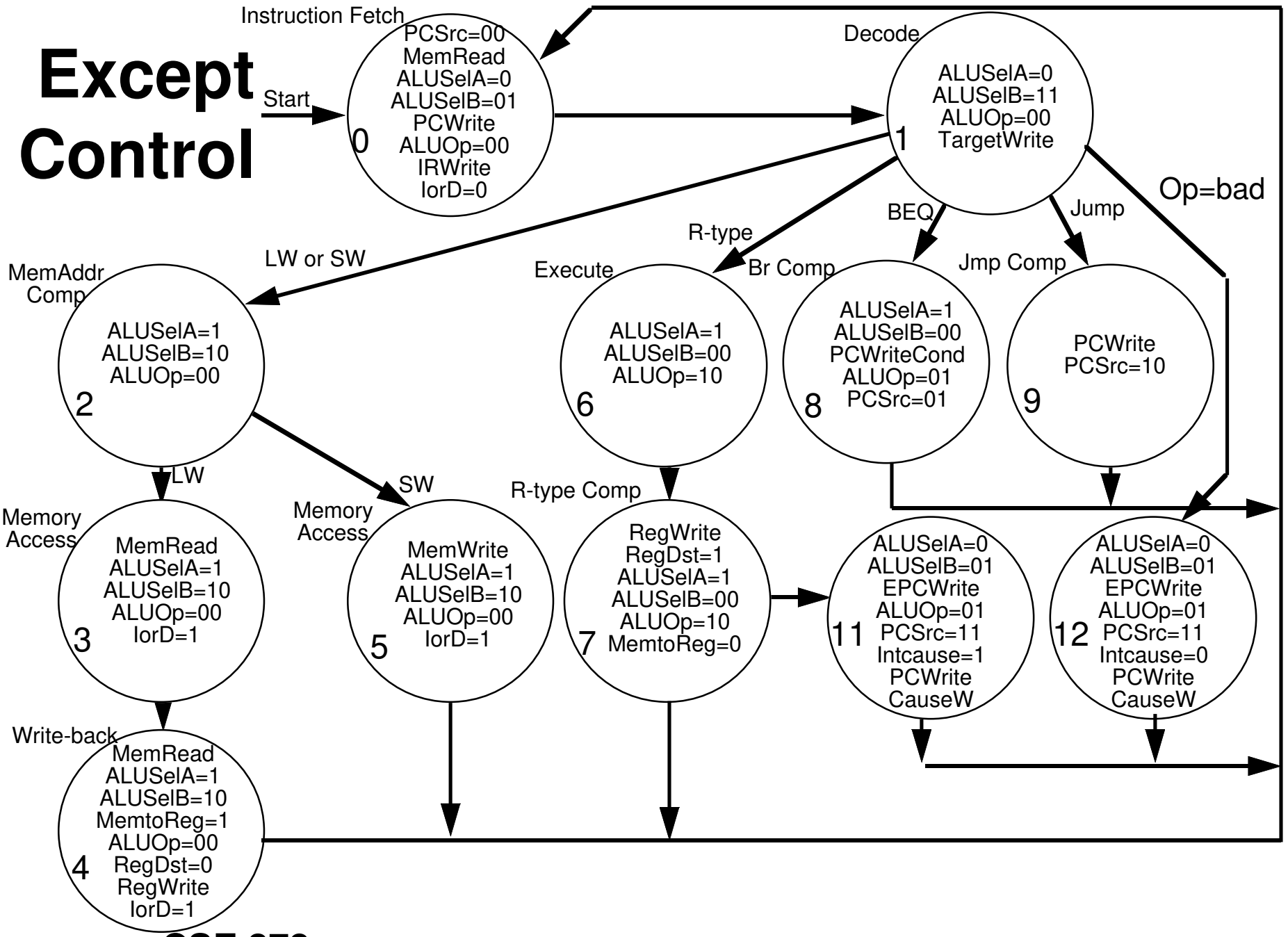
Except Control



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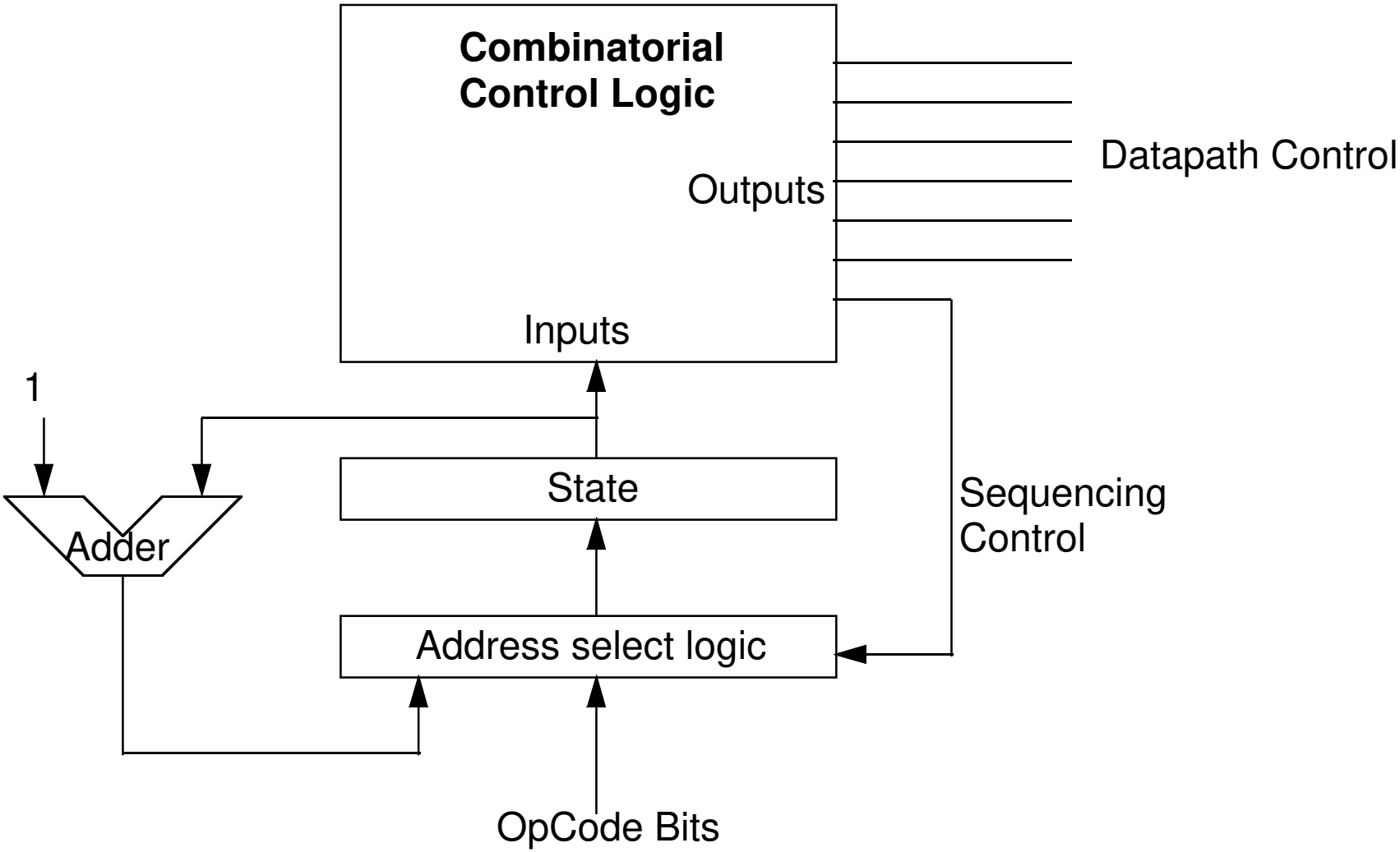
Microcode



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A Microinstruction Format

Field Name	Function of Field	Values
ALU Control	Configure the ALU	Add / Funct / Sub
SRC1	First ALU operand	PC / rs
SRC2	Second ALU operand	4 / Extend / Extshift / rt
ALU Dest	Reg to be written w/ALU result	Target / rd
Memory	Specify R/W & Address source	ReadPC / ReadALU / WriteALU
Memory Reg	Destination/Source of Memdata	IR / Write rt / Read rt
PCWrite Ctl	Specify writing to PC	ALU / Target-cond / jump addr
Sequencing	How to chose next microinst	Seq / Fetch / Dispatch1

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The Microprogram

Label	ALU Control	SRC1	SRC2	ALU Destin	Mem	Mem Register	PC Write Ctl	Seq
Fetch	Add	PC	4		Read PC	IR	ALU	Seq
	Add	PC	Extshift	Target				Disp 1
LWSW1	Add	rs	Extend					Disp 2
LW2	Add	rs	Extend		ReadALU			Seq
	Add	rs	Extend		ReadALU	Write rt		Fetch
SW2	Add	rs	Extend		WriteALU	Read rt		Fetch
R-fmt	Funct	rs	rt					Seq
	Funct	rs	rt	rd				Fetch
BEQ1	Sub	rs	rt				Target	Fetch
Jump1							Jump	Fetch

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