

Lecture 7

- HW1 due Wednesday
- Machine language, the binary representation for instructions.
 - I-type, immediates
 - J-type, surprise
 - Encoding
- Strlen example?

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R-type format

- Register-to-register arithmetic instructions use the R-type format.

op	rs	rt	rd	shamt	func
6 bits	5 bits	5 bits	5 bits	5 bits	6 bits

- This format includes six different fields.
 - op is an operation code or opcode that selects a specific operation.
 - rs and rt are the first and second source registers.
 - rd is the destination register.
 - shamt is only used for shift instructions.
 - func is used together with op to select an arithmetic instruction.
- The green card in the textbook lists opcodes and function codes for all of the MIPS instructions.

$$add: R[rd] = R[rs] + R[rt]$$

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About the registers

- We have to encode register names as 5-bit numbers from 00000 to 11111.
 - For example, \$t8 is register \$24, which is represented as 11000.
 - The complete mapping is given on page B-24 in the book.
- The number of registers available affects the instruction length.
 - Each R-type instruction references 3 registers, which requires a total of 15 bits in the instruction word.
 - We can't add more registers without either making instructions longer than 32 bits, or shortening other fields like op and possibly reducing the number of available operations.

op	rs	rt	rd	shamt	func
6 bits	5 bits	5 bits	5 bits	5 bits	6 bits

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I-type format

- Load, store, branch, and immediate instructions all use the I-type format.

op	rs	rt	address
6 bits	5 bits	5 bits	16 bits

- For uniformity, op, rs and rt are in the same positions as in the R-format.
- The meaning of the register fields depends on the exact instruction.
 - rs is a source register—an address for loads and stores, or an operand for branch and immediate arithmetic instructions.
 - rt is a source register for branches and stores, but a destination register for the other I-type instructions.
- The address is a 16-bit signed two's-complement value.
 - It can range from -32,768 to +32,767.
 - But that's not always enough!

$$R[rt] = R[rs] + imm$$

lw R[rt] = {imm, 16 bits}

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Larger constants

- Larger constants can be loaded into a register 16 bits at a time.
 - The load upper immediate instruction lui loads the highest 16 bits of a register with a constant, and clears the lowest 16 bits to 0s.
 - An immediate logical OR, ori, then sets the lower 16 bits.
- To load the 32-bit value 0000 0000 0011 1101 0000 1001 0000 0000:

```
lui $s0, 0x003D # $s0 = 003D 0000 (in hex)
ori $s0, $s0, 0x0900 # $s0 = 003D 0900
```

- This illustrates the principle of making the common case fast.
 - Most of the time, 16-bit constants are enough.
 - It's still possible to load 32-bit constants, but at the cost of two instructions and one temporary register.
- Pseudo-instructions may contain large constants. Assemblers including SPIM will translate such instructions correctly.

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Two's complement (reminder)

- Easy to do in HW
 - Most significant bit tells sign (sign bit)
 - Addition can be done without anything special
- How?
 - Invert all bits and add one

8-bit two's-complement integers	
0 1 1 1 1 1 1 1 = 127	
0 0 0 0 0 0 1 0 = 2	
0 0 0 0 0 0 0 1 = 1	
0 0 0 0 0 0 0 0 = 0	
1 1 1 1 1 1 1 1 = -1	
1 1 1 1 1 1 1 0 = -2	
1 0 0 0 0 0 0 1 = -127	
1 0 0 0 0 0 0 0 = -128	

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Loads and stores

- The limited 16-bit constant can present problems for accesses to global data.
- Suppose we want to load from address 0x10010004, which won't fit in the 16-bit address field. Solution:

```
lui $at, 0x1001      # 0x1001 0000
lw  $t1, 0x0004($at) # Read from Mem[0x1001 0004]
```

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Branches

- For branch instructions, the constant field is not an address, but an *offset* in words from the current program counter (PC) to the target address.

```

-> beq $at, $0, L
1 add $v1, $v0, $0
2 add $v1, $v1, $v1
3 j  somewhere
L: add $v1, $v0, $v0

```

*PC = PC + 3 * 4*

- Since the branch target L is three instructions past the beq, the address field would contain 3. The whole beq instruction would be stored as:

000100	00001	00000	0000 0000 0000 0011
op	rs	rt	address

- For some reason SPIM is off by one, so the code it produces would contain an address of 4. (But SPIM branches still execute correctly.)

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Larger branch constants

- Empirical studies of real programs show that most branches go to targets less than 32,767 instructions away—branches are mostly used in loops and conditionals, and programmers are taught to make code bodies short.
- If you do need to branch further, you can use a jump with a branch. For example, if “Far” is very far away, then the effect of:

```
beq $s0, $s1, Far
...
```

can be simulated with the following actual code.

```
bne $s0, $s1, Next
j   Far
Next: ...
```

- Again, the MIPS designers have taken care of the common case first.

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J-type format

- Finally, the jump instruction uses the J-type instruction format.

absolute

op	address
6 bits	26 bits

PC = lium << 2

- The jump instruction contains a *word address*, not an offset.
 - Remember that each MIPS instruction is one word long, and word addresses must be divisible by four.
 - So instead of saying “jump to address 4000,” it’s enough to just say “jump to instruction 1000.”
 - A 26-bit address field lets you jump to any address from 0 to 2²⁶.
 - your MP solutions had better be smaller than 256MB

- For even longer jumps, the jump register, or jr, instruction can be used.

```
jr $ra # Jump to 32-bit address in register $ra
```

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Summary of Machine Language

- Machine language is the binary representation of instructions:
 - The format in which the machine actually executes them
- MIPS machine language is designed to simplify processor implementation
 - Fixed length instructions
 - 3 instruction encodings: R-type, I-type, and J-type
 - Common operations fit in 1 instruction
 - Uncommon (e.g., long immediates) require more than one

R	opcode	rs	rt	rd	shamt	funct
I	opcode	rs	rt	immediate		
J	opcode	target address				

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Decoding Machine Language

How do we convert 1s and 0s to assembly language and to C code?

Machine Language → assembly → C?

For each 32 bits:

- Look at opcode to distinguish between R-Format, JFormat, and I-Format
- Use instruction format to determine which fields exist
- Write out MIPS assembly code, converting each field to name, register number/name, or decimal/hex number
- Logically convert this MIPS code into valid C code. Always possible? Unique?

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Decoding (7/7)

- Possible C code:

```
$v0: var1
$a0: var2
$a1: var3
var1 = 0;
while (var3 >= 0) {
    var1 += var2;
    var3 -= 1;
}
```

```
or      $v0,$0,$0
Loop:  stl   $t0,$0,$a1
      beq   $t0,$0,Exit
      add  $v0,$v0,$a0
      addi $a1,$a1,-1
      j    Loop
Exit:
```

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strlen Example

```
void somefunc() (
    char *str;
    int a;
    /*uses t0, t1 somewhere */
    -
    a = strlen(str);
    -
}

int strlen(char *str) (
    int count = 0;
    while (*s != 0) {
        count++;
        s++;
    }
    return count;
}
```

caller-saved: \$t0-\$t9, \$a0-\$a9, \$v0-\$v9, callee-saved: \$s0-\$s7, \$ra

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strlen Example

```
void somefunc() (
    char *str;
    int a;
    /*uses t0, t1 somewhere */
    -
    a = strlen(str);
    -
)

somefunc:
    addi $sp, $sp, -12
    sw   $ra, 0($sp)
    sw   $t0, 4($sp)
    sw   $t1, 0($sp)
    add  $a0, $t0, $0
    jal  strlen
    lw   $t1, 0($sp)
    lw   $t0, 4($sp)
    lw   $ra, 0($sp)
    addi $sp, $sp, 12
    jr   $ra

int strlen(char *str) (
    int count = 0;
    while (*s != 0) {
        count++;
        s++;
    }
    return count;
)

strlen:
    addi $t0, $0, 0
    loop:
        lb  $t1, 0($t0)
        beq $t1, $0, end_loop
        addi $t0, $t0, 1
        addi $t1, $t1, 1
        j   loop
    end_loop:
        add  $v0, $t0, $0
        jr  $ra
```

caller-saved: \$t0-\$t9, \$a0-\$a9, \$v0-\$v9, callee-saved: \$s0-\$s7, \$ra

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