1. 1100 0101 0101 0110 1010 1100 0100 0100
2. 3AA953BC
3. sign: 0 exponent: 011 1010 1 fraction: 010 1001 0101 0011 1011 1100
4. 1023
5. 2^{n-1}-1 or 0 followed by n-1 1s
6. jr $ra or jr $31
7. lui $t1, 0x5555 #load top bits of mask
   ori $t1, 0x5555 #add on the bottom bits
   and $t0, $t0, $t1 #save odd bits
8. add $result, $source, $0
   setl $at, $result, $0
   beq $at, skip1
   sub $result, $0, $result

skip1:

9. The low order bit in $t0 is 0 because it is halfword aligned
10. sll $t0, $a1, 2 #multiply index by 4
    add $t1, $t0, $a0 #figure A[n] address
    lw $t2, 0($t1) #save in t2 temp

loop: beq $t1, $a0, exit #done? yes, so long
      lw $t5, -4($t1) #grab val on left
      sw $t5, 0($t1) #shift it right
      addi $t1, $t1, -4 #decrement address
      j loop #iterate

exit: sw $t2, 0($t1) #put A[n] at front

11. lw $t0, 0($sp)
    addi $t0, -1
    sw $t0, -4($sp)
    addi $sp, $sp, -4

12. beq, bne, j, jal
13. <<show colors>>
14. ALUSrc = 0, ALUOp = 010 or add, MemWrite = 1
15. <<show colors>>
16. Single Cycle: 10+1+2+10+1 = 24 Multicycle: 10